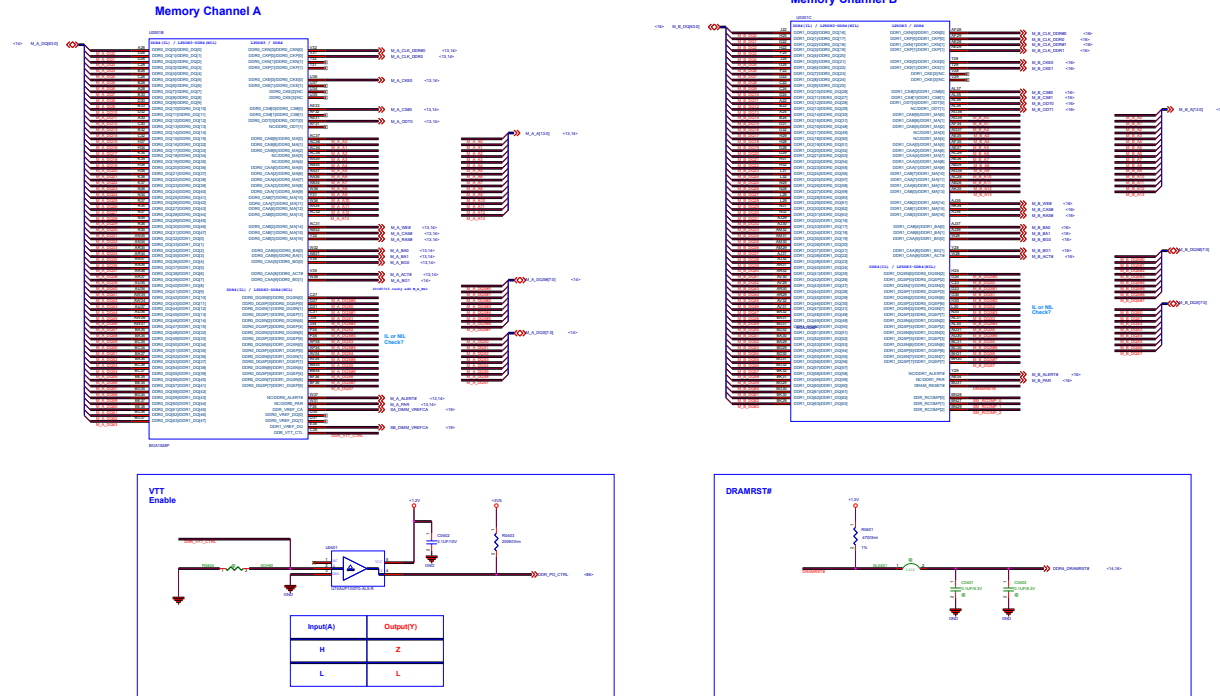
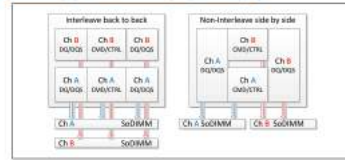
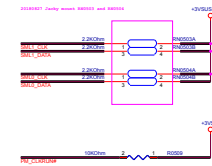
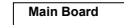
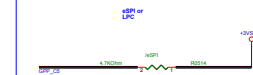


Figure 2-2. Interleave (IL) and Non-Interleave (NIL) Modes Mapping





GPP_B23 (Internal DCI-DOE) Function	Intel DCI-DOE	Intel Internal DCI-DOE
		The signal has an internal pull-down.
		0 = signal brought low by the pull-down
		1 = signal brought high by the pull-up
		Note:
		1. The internal pull-down is disabled after 150MHz operation.
		2. The signal is not sampled by the internal DCI-DOE function. It is sampled by the external DCI-DOE function.
		This signal is on the private rail.



This signal has a weak internal pull-down.

- 0 = LPC is selected (for EC). (Default)
- 1 = eSPI is selected (for EC).

Notes:

1. The internal pull-down is disabled after RSNRST# de-asserts.
2. The signal is in the primary well.

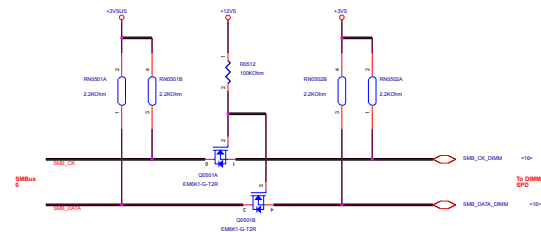
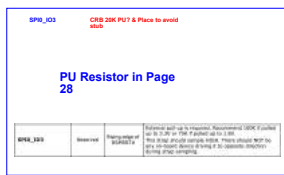
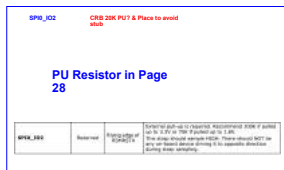
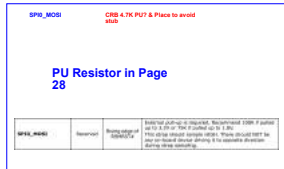
Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled).

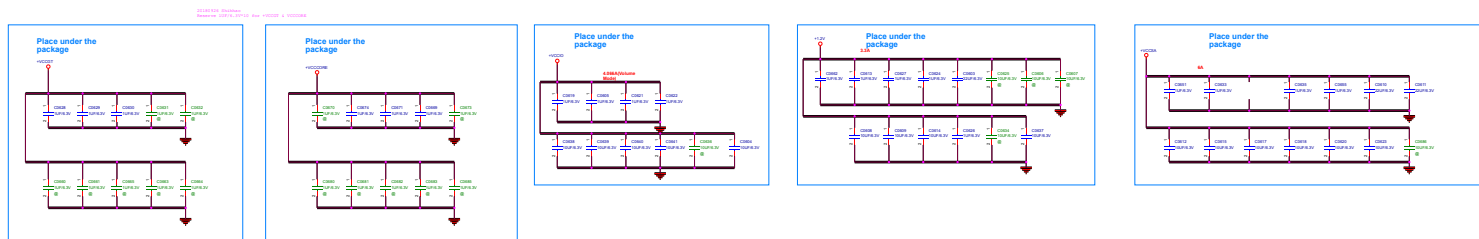
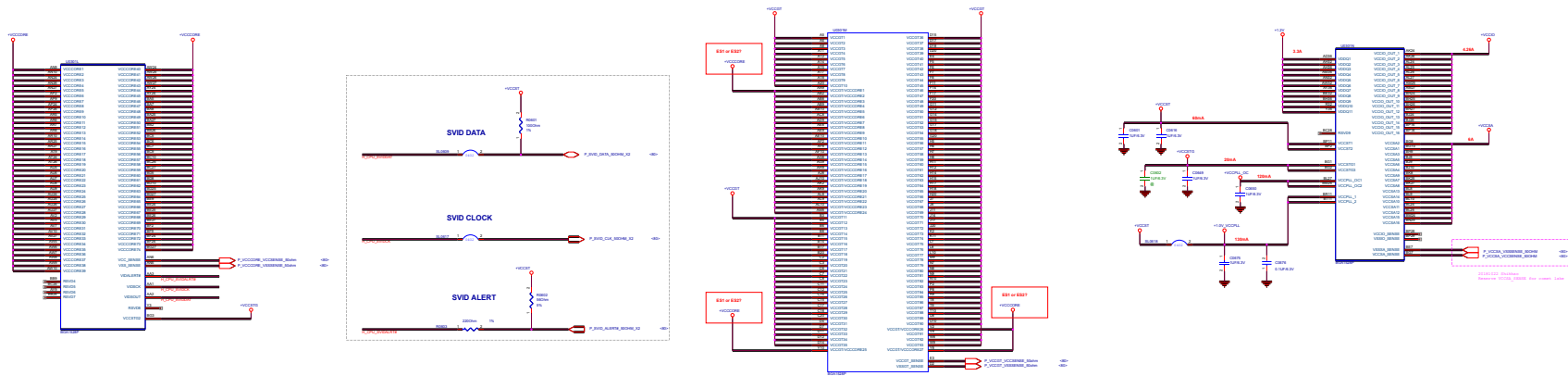


GPP_C2: weak internal pull down	
PU	Enable (to support Intel AMT with TLS)
PD	Disable Intel ME TLS other suite (no confidentiality)(Default)

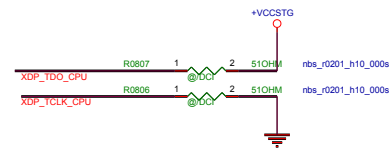
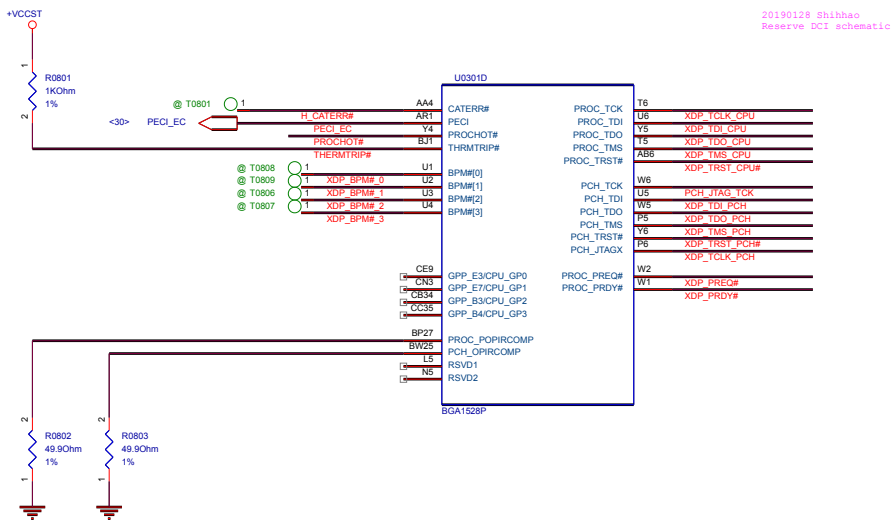
- This signal has a weak internal pull-down.
- 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
- 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
- Notes:**
1. The internal pull-down is disabled after RSMRST# de-asserts.
 2. This signal is in the primary well.

		Project Name		Rev
X409F				R1.0
Title : CPU_LPC, SPI, SMBus, CLINK				
Size	Dept.: ASUSTek		Engineer: NB3EE2	
C	Date: Friday, February 22, 2019		Sheet	5 of 101





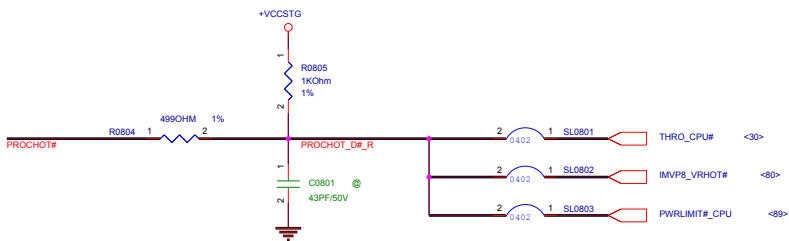
Main Board



TP for Boundary Scan Test



PU Power change from VCCIO to VCCSTG



From EC (by Thermal Sensor)

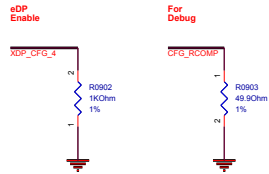
OD Gate (100ohm PD)

OD Gate (100ohm PD)

ASUS		Project Name	Rev
X409F			R1.0
Title : CPU_MISC,ITAG			
Size	Dept.:	ASUSTek	Engineer: NB3EE2
B	Date: Friday, February 22, 2019	Sheet 8	of 101

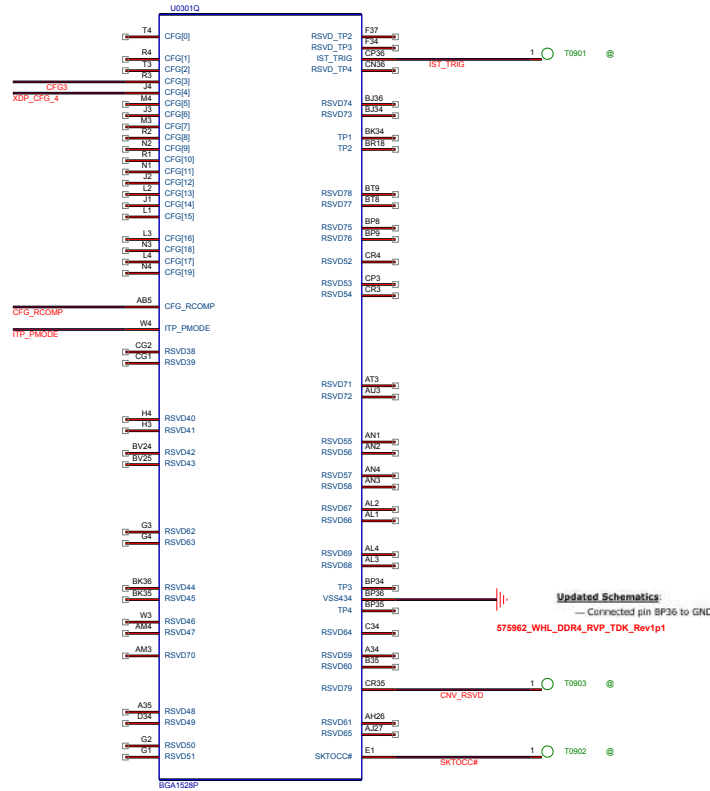
TP for Boundary Scan Test

TPC28T_50 1 T0910 CFG3
TPC28T_50 1 T0911 ITP_PMODE



	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

CFG0	Stall reset sequence after PCU PLL lock until de-asserted	Connect a series 1 KOhm resistor on the critical CFG0 trace in a manner which does not introduce any stubs to CFG0 trace. Route as needed from the opposite side of this series isolation resistor to the above port. TTP will drive the net to GND.
------	---	--



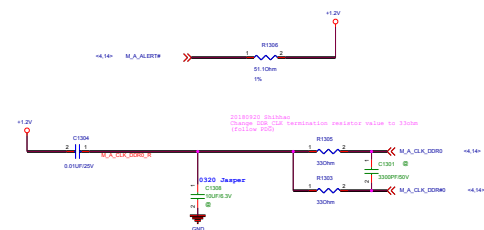
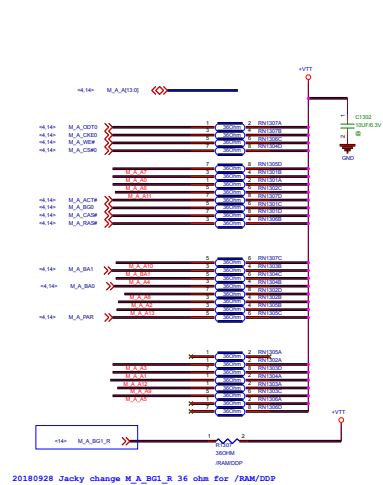
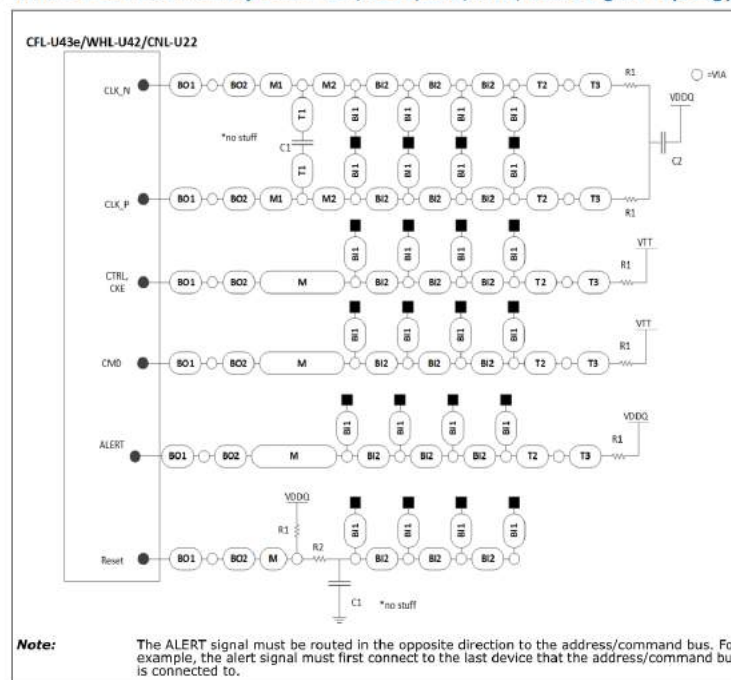
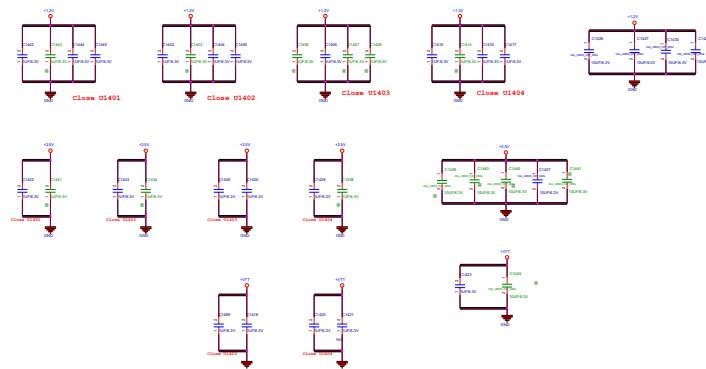
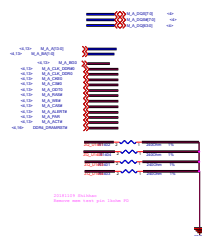
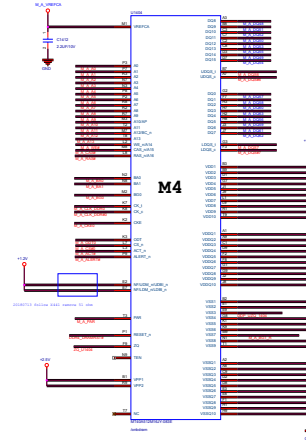
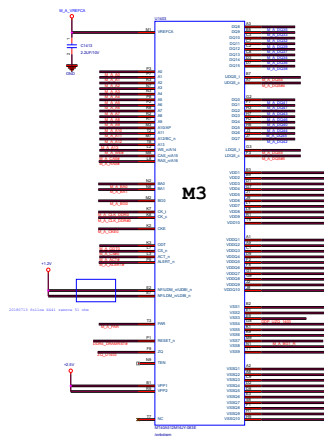
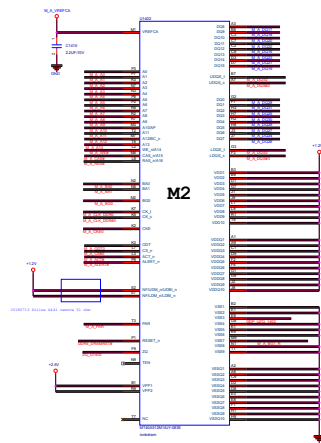
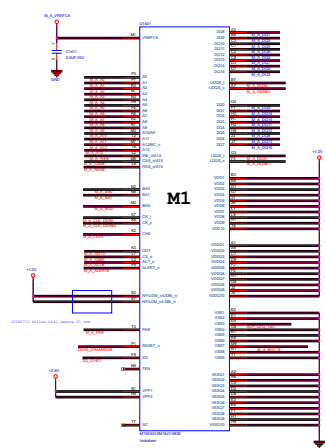
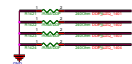
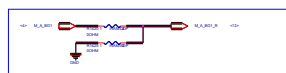


Figure 4-7. WHL U DDR4 x16 Memory Down CLK/CTRL/CKE/CMD/Reset Signal Topology

Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS# [3:0], ODT[3:0]	CS# [3:0], ODT[3:0]	CS# [1:0], ODT[1:0]	CS# [1:0], ODT[9]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[3:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[0], DQSN[0]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]





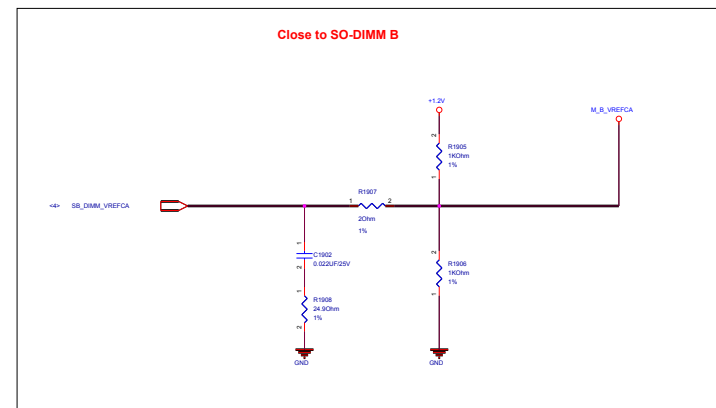
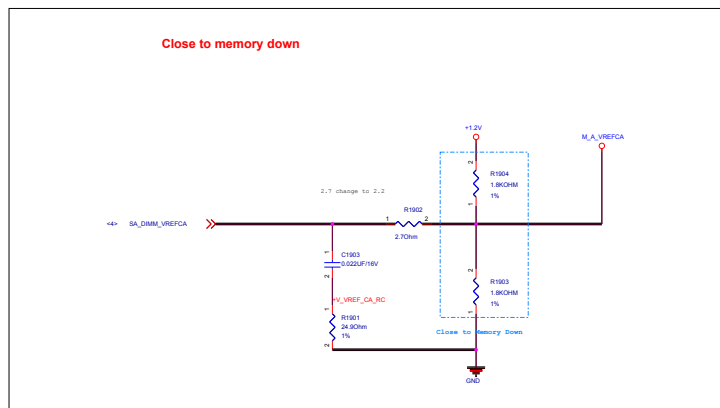
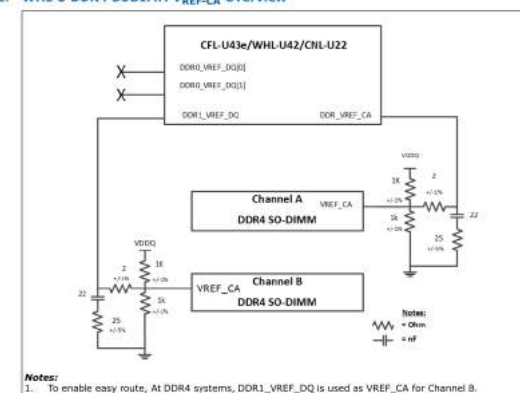
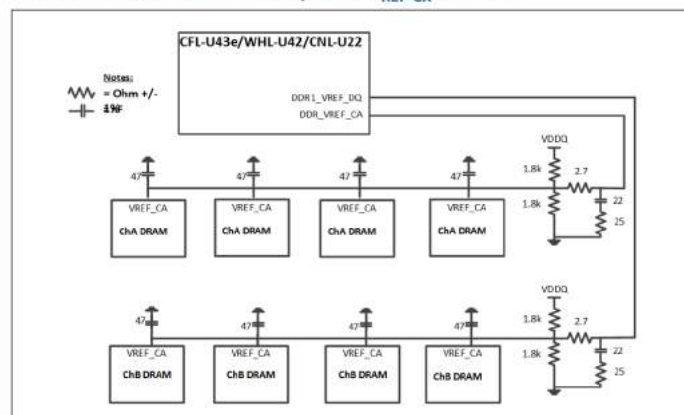


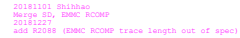
Figure 4-1. WHL U DDR4 SODIMM V_{REF-CA} Overview

Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

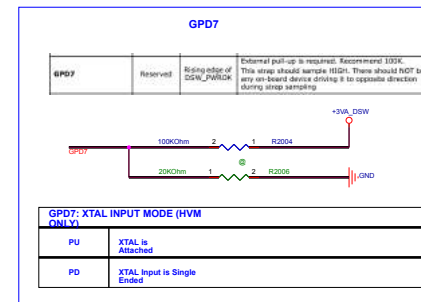
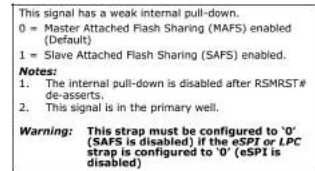
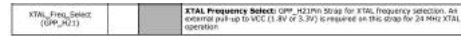
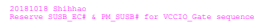


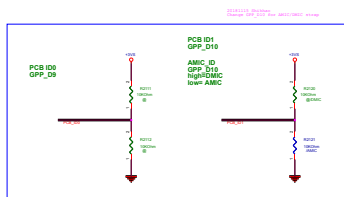
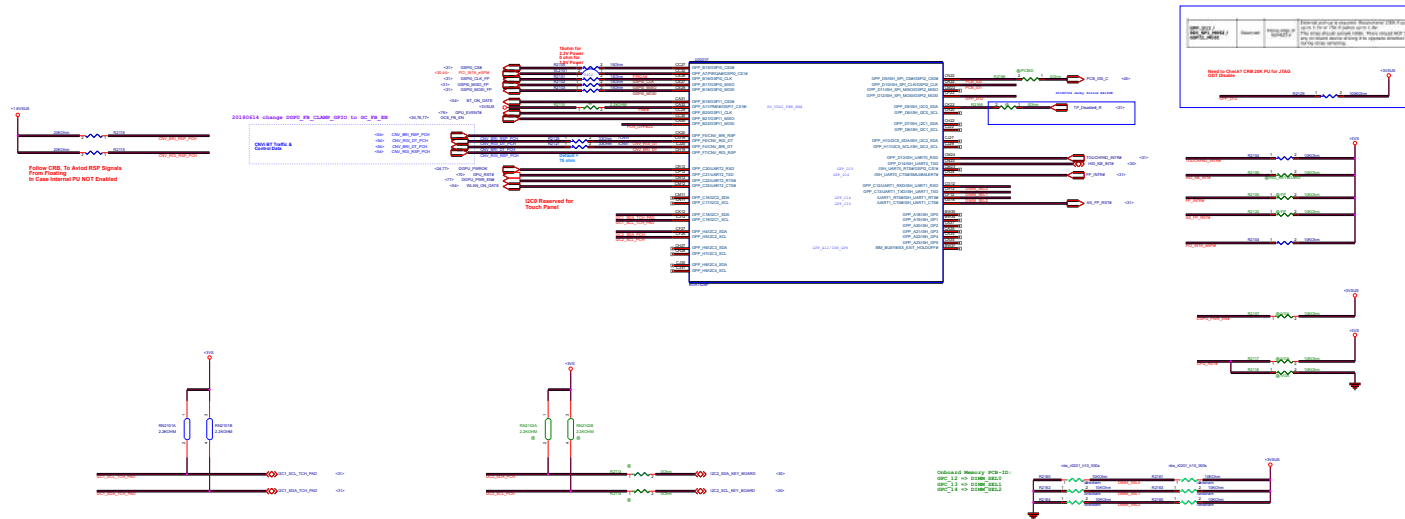
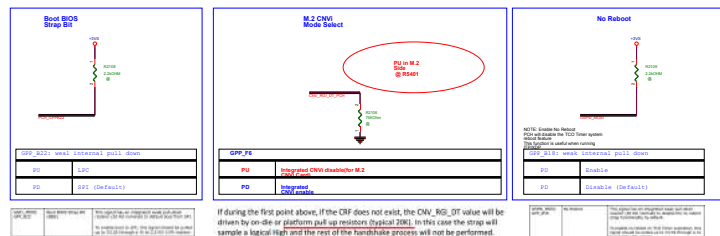
Project Name		Rev
ASUS X409F		R1.0
Title : DORA_CA,DQ_VREF		
Size	Dept.: ASUS/STW	Engineer: NB3EE2
Customer	Date: Friday February 22, 2019	Sheet 10 of 101

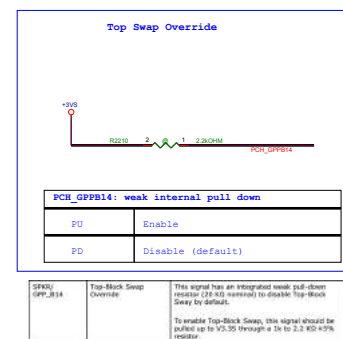
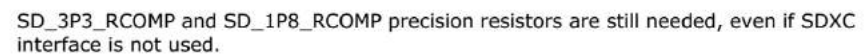
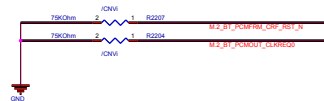
The During Reset Pin State of this GPIO is H via a $\sim 20\text{k}\Omega$ pull-up to 3.3 V independent of soft strap assigned pad voltage. A 1.8 V device connected to this GPIO must be capable of taking $\sim 20\text{k}\Omega$ pull-up to 3.3 V.



Note:

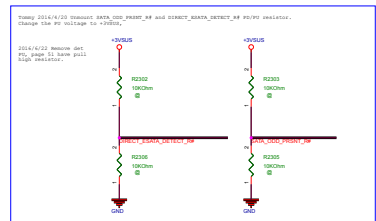


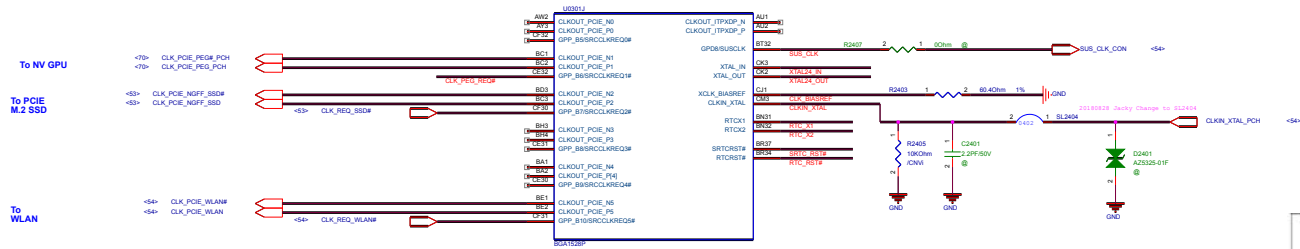
[illegible]



PCle Controller 1#	1	USB1_P0R1 TYPE-A
	2	USB1_P0R1 TYPE-A
	3	USB1_P0R1 TYPE-A
	4	USB1_P0R1 TYPE-A
PCle Controller 2#	5	GP1 IO_Lane0
	6	GP1 IO_Lane1
	7	GP1 IO_Lane2
	8	GP1 IO_Lane3
PCle Controller 3#	9	WLAN BT
	11	RAJAL_J202
	12	DATA_M2_2 (SATA/USB/PCIe)
	13	POBERRATA_M2_2002_2 (eMMC)
PCle Controller 4#	14	POBERRATA_M2_2002_2 (eMMC)
	15	POBERRATA_M2_2002_2 (eMMC)
	16	POBERRATA_M2_2002_2 (eMMC)

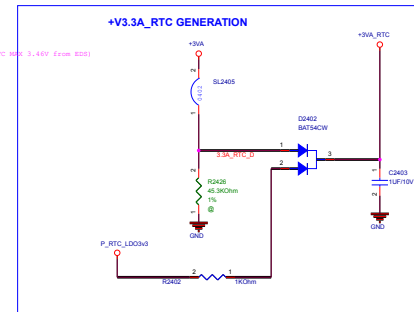
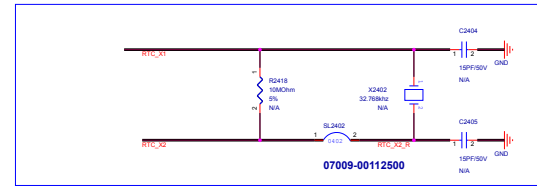
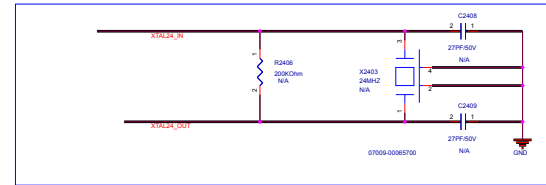
USB		USB	
1	USB 1.0 Port type-A	USB_1	USB 3.1 GEN-1 type-A (SW Charger)
2	IO USB2.0 Port	USB_2	
3	USB 3.0 Port type-C	USB_3	USB 3.1 GEN-1 type-C
4	Card Reader	USB_4	USB 3.1 GEN-1 type-C
5	Camera		
6	IO USB2.0 Port		
7	N/A		
8	N/A		
9	N/A		
10	BT		



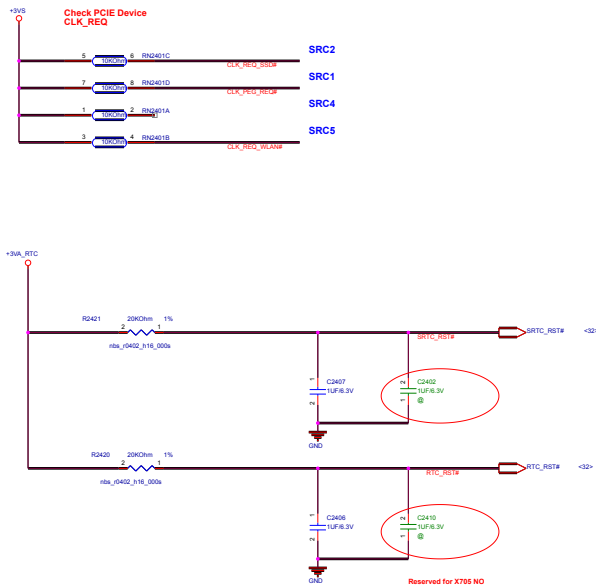


53	SUSCLK	Slow clock input for low power logic. Connect to a 32KHz clock from the Platform or SOC.	Optional Slow clock input for the power logic. Connect to a 32KHz clock from the Platform or SOC. This clock may not be required, depending on the R.P. module specific requirements.
----	--------	--	---

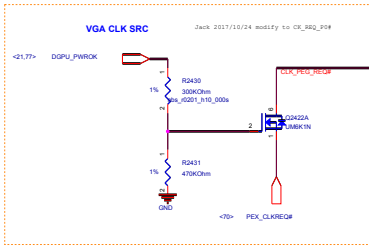
20180821 Jacky follow X705PD



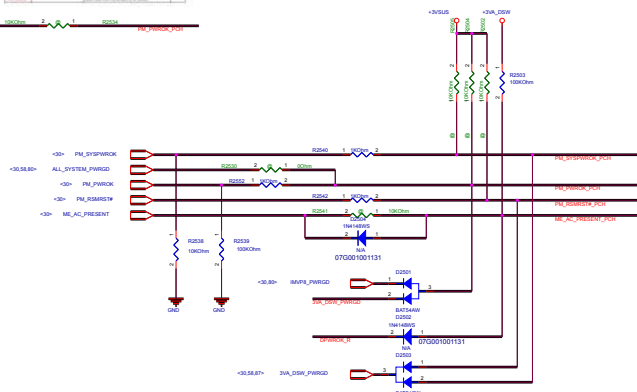
20180914: 01100000
Change R2402 to 10k to support R2402 (RTC) with 3.3V (from 0001)

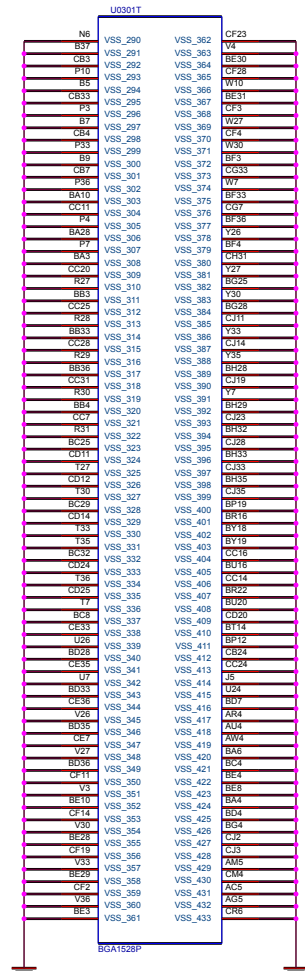
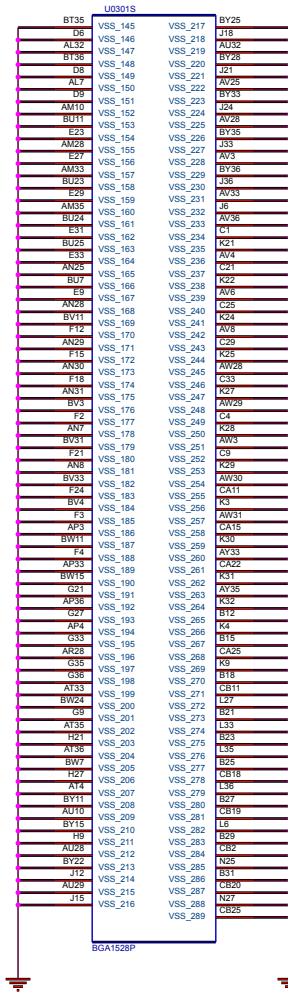
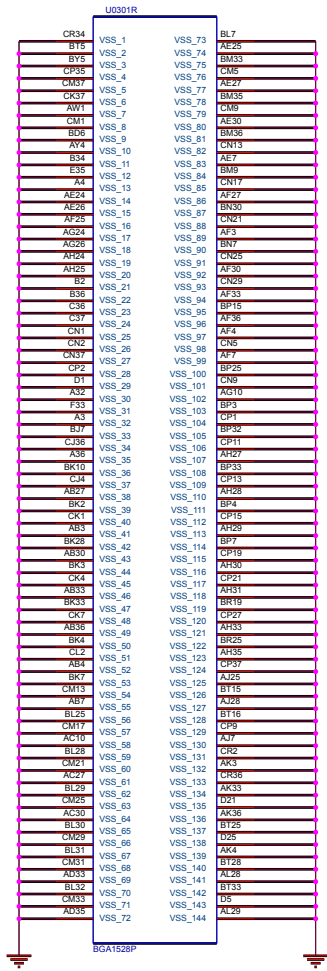


20180614 Jacky follow UX530



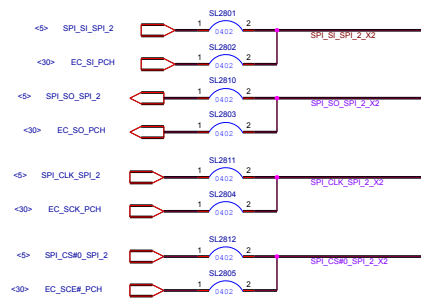
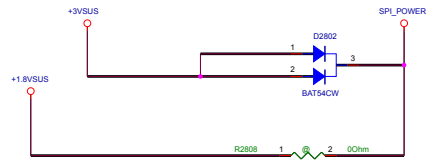
RTCEN1#		An RC delay circuit with a time delay in the range of 10-25 ms should be provided. The recommended values for resistor and capacitor are 20kΩ and 1.0μF. The circuit should be connected to V3.3V.
RTCEN2#		An RC delay circuit with a time delay in the range of 10-25 ms should be provided. The recommended values for resistor and capacitor are 20kΩ and 1.0μF. The circuit should be connected to V3.3V.



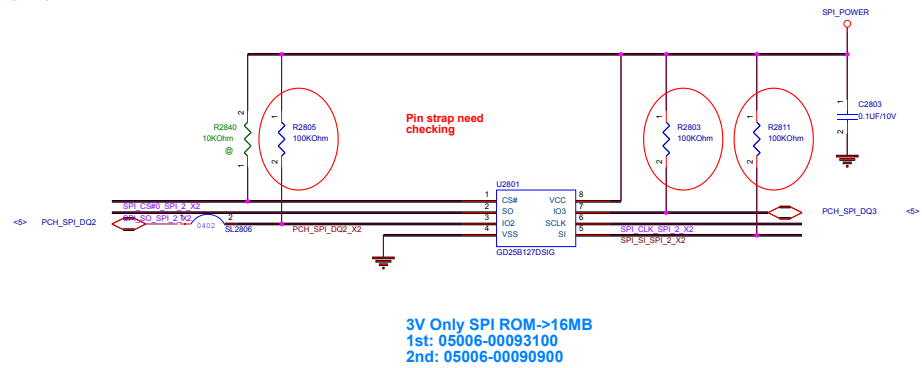


Project Name		Rev
ASUS X409F		R1.0
Title : CPU_PCH_GND		
Size	Dept.:	Engineer:
B	ASUSTek	NB3EE2
Date: Friday, February 22, 2019	Sheet	27 of 101

SPI PCH Power

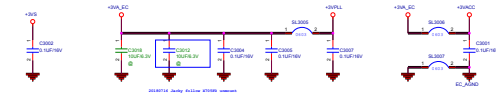


3V SPI ROM For WHL (16MB)

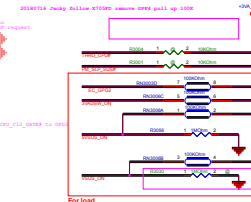
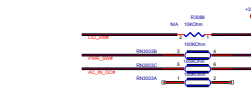
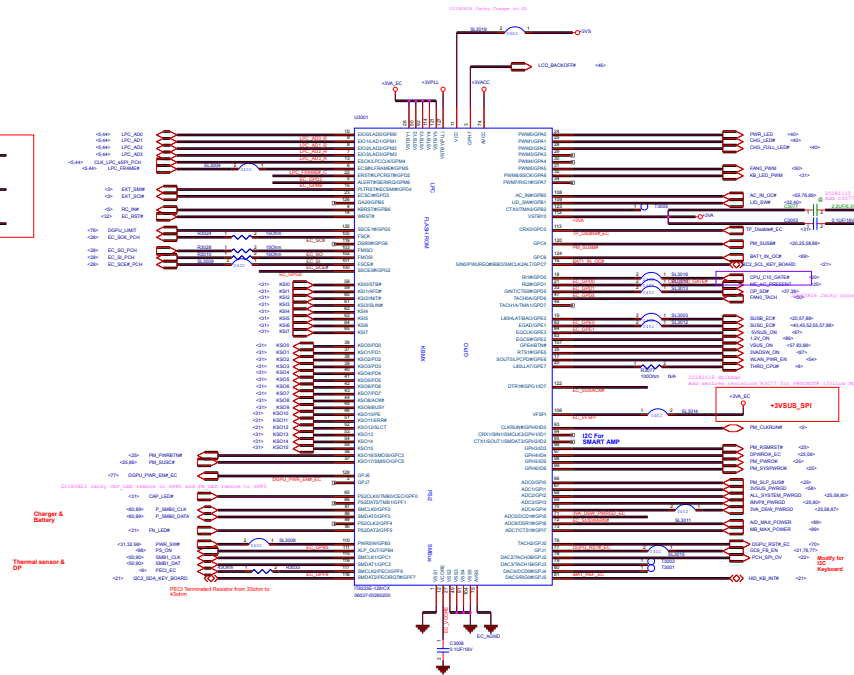
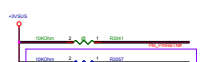
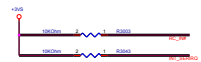


ASUS		Project Name	Rev
X409F			R1.0
Title : PCH-SPI ROM			
Size	Dept.: ASUSTek	Engineer: NB3EE2	
A3			
Date: Friday, February 22, 2019		Sheet	28 of 101

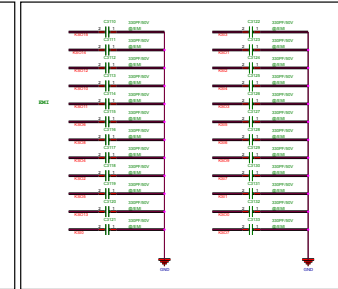
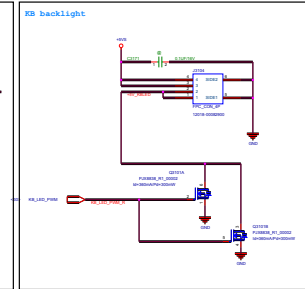
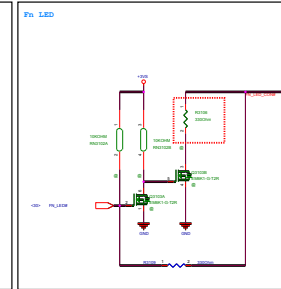
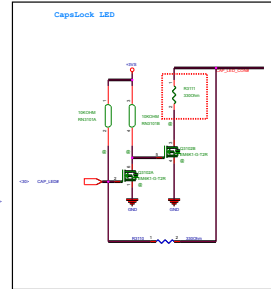
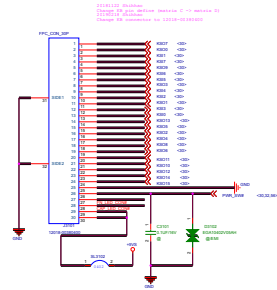
Power



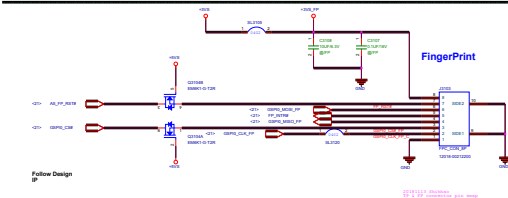
Note: BERRQ pin share with VFSPI Power(3.3V or 1.8V)



Internal Keyboard

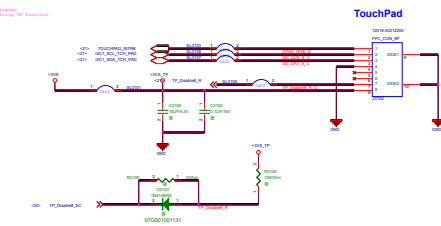


Main Board



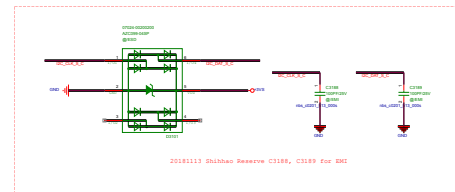
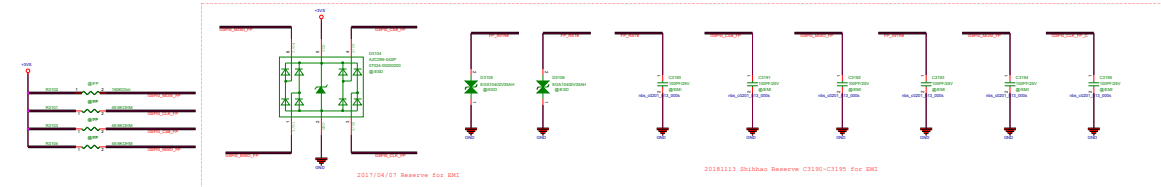
Follow Design

20181113 Shihao
20181113 Shihao Reserve C190-C195 for DMC
Design 18 10/10/18

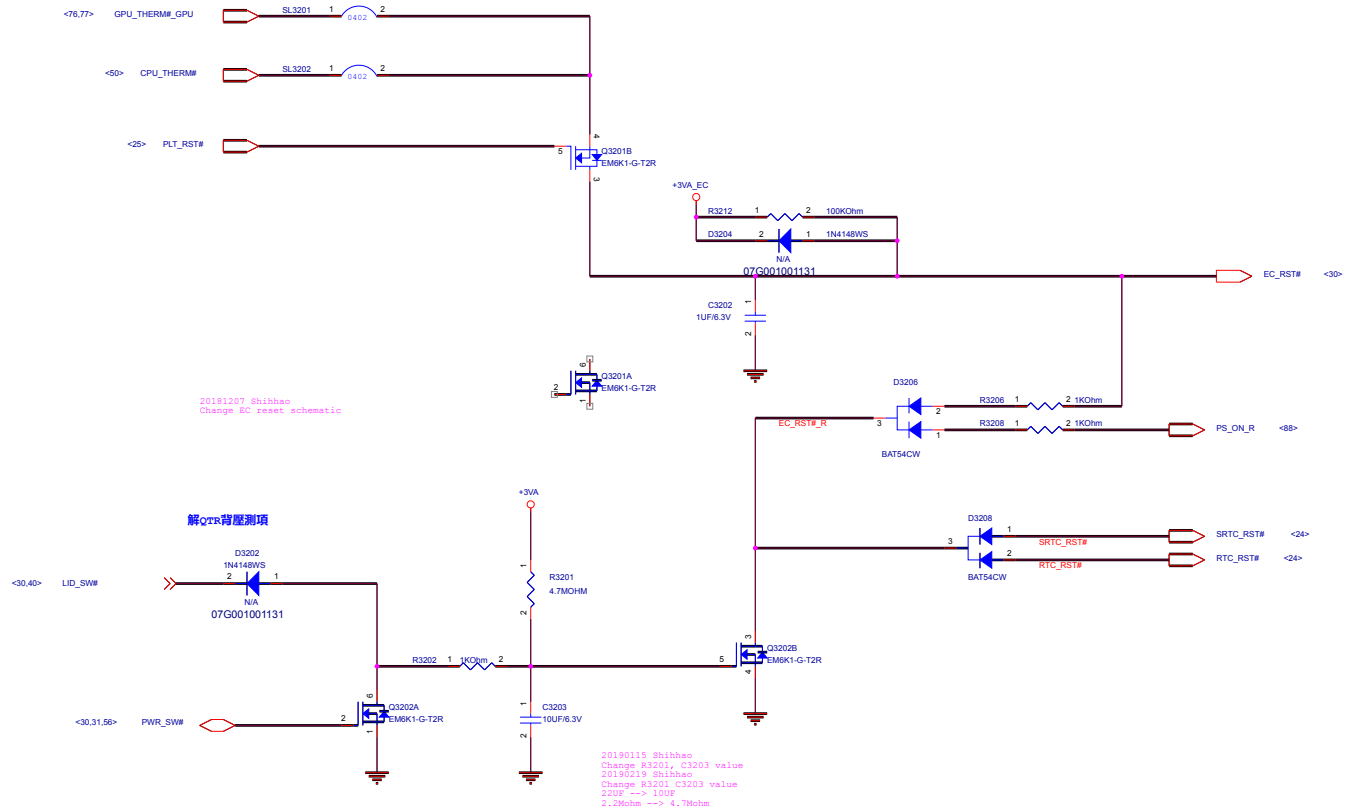


USB Finger printer (Reserved)

Pin	Pin	Pin	Pin
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24



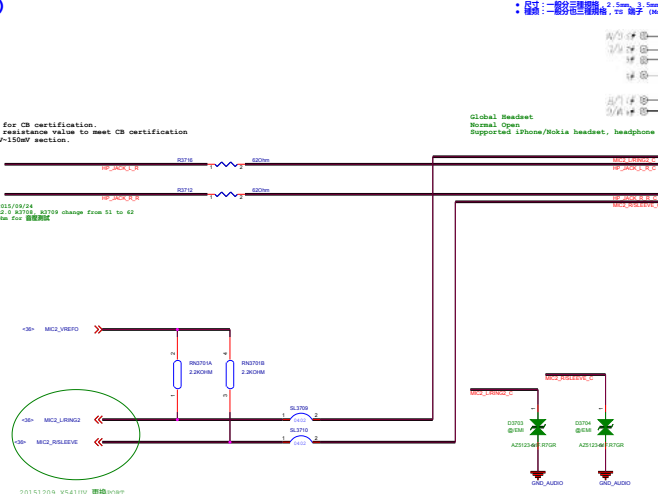
Pin	Pin	Pin	Pin
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24



Universal Jack (Normal open type)

R1.3, Item 12:
Add 4 pole headset jack normal open type for project demand.

R1.4, Item 13:
Recommend the SP damping resistance 56 ohm for CB certification.
Depend on your project, you can change the resistance value to meet CB certification (under 1500W). Best choice is between 140W-150W section.



• 耳机：一般分三种规格：4.5mm, 3.5mm, 6.35mm
• 规格：二极分压电阻器，2W 端子 (Stereo), 3W 端子 (Stereo + Mic/Video),

Global Headset
Normal Open
Supported iPhone/Nokia headset, headphone

CITA: 國際標準

Apple iPhone/iPad/小米 的 Phone Jack 定義:

Apple	IPad (Stereo)	iPod (Stereo)	iPhone (Mic)	iPod (AV)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	Ground	Ground	Mic	Video
4. Sleeve	Ground	Ground	Ground	Ground

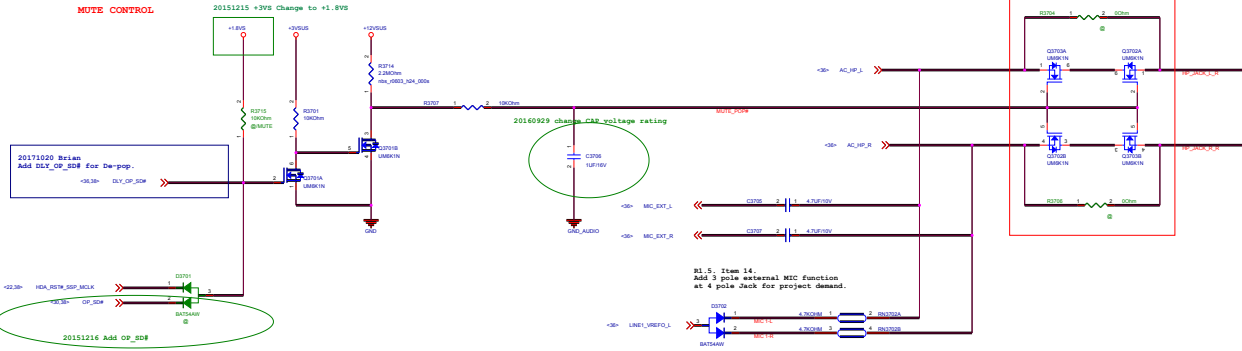
CMPT: 國家標準

Nokia Type 的 Phone Jack 定義:

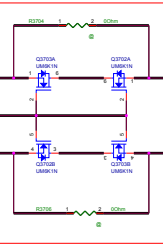
Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel



耳機pop noise mute線路
MUTE CONTROL



MUTE CONTROL

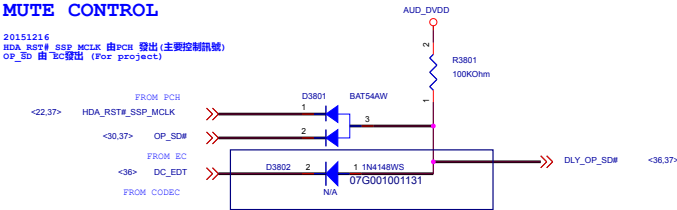


R1.5, Item 14:
Add 3 pole external MIC function at 4 pole Jack for project demand.

20160530
1. Del R3833 & Add D3801
2. AUD_DVDD_IO--->AUD_DVDD

MUTE CONTROL

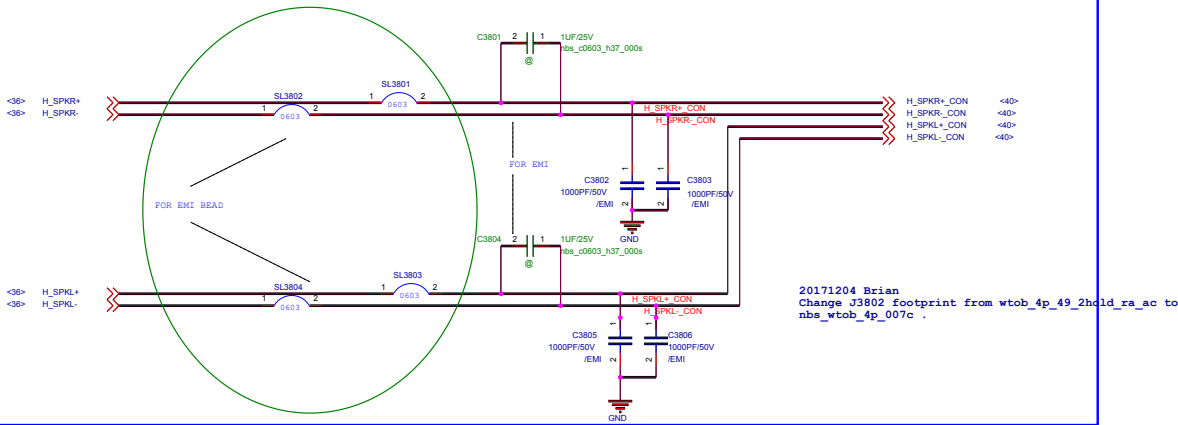
20151216
HDA_RST#_SSP_MCLK 由PCH 發出 (主要控制信號)
OP_SD 由 IC 發出 (For project)



20171020 Brian
Change R3833 to D3802 for De-pop.

Trace width for
H_SPKL+ O/H SPKL- O/H SPKR+ O/H SPKR- OSpeaker
Speaker : 4 ohm : 40mil ; 8 ohm : 20mil

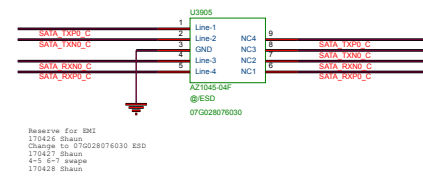
20180828 Jacky Change C3802,C3803,C3805,C3806 to 1000pF and mount them



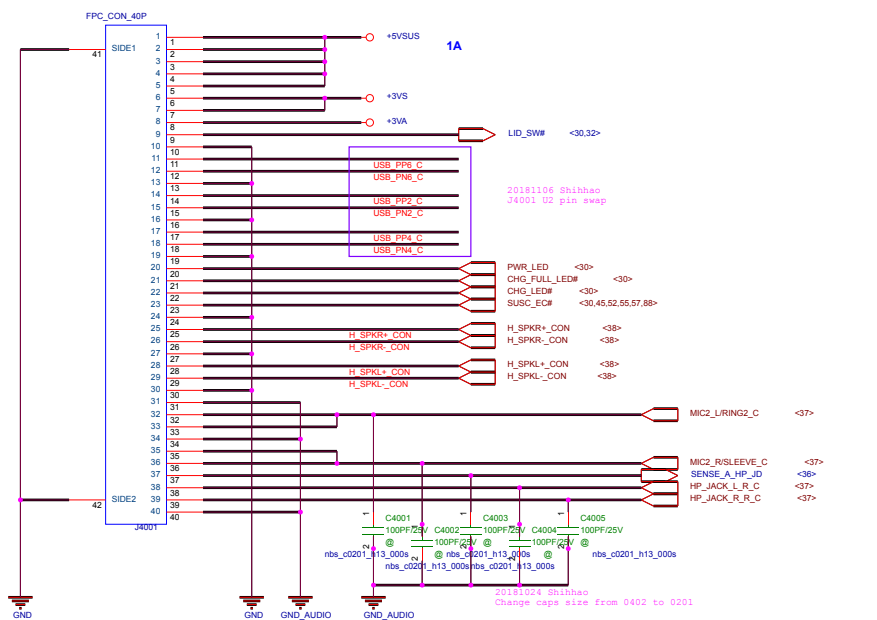
20171204 Brian
Change J3802 footprint from wtob_4p_49_2hold_ra_ac to nbs_wtob_4p_007c .

[illegible][illegible]

FFC	PIN	DEFINE	SATA CONN
		GND	P11
		GND	P10
1	E	5V	P9
2		5V	P8
3		5V	P7
		GND	P6
		GND	P5
		GND	P4
4		GND	S7
5		RXP(B→)	S6
6		RXNC(B→)	S5
7		GND	S4
8		TXNCA(→)	S3
9		TXPCA(→)	S2
10		GND	S1

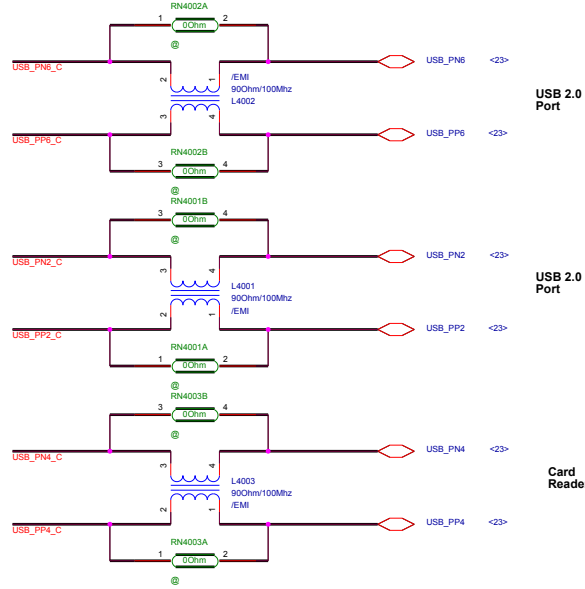


MB to IO



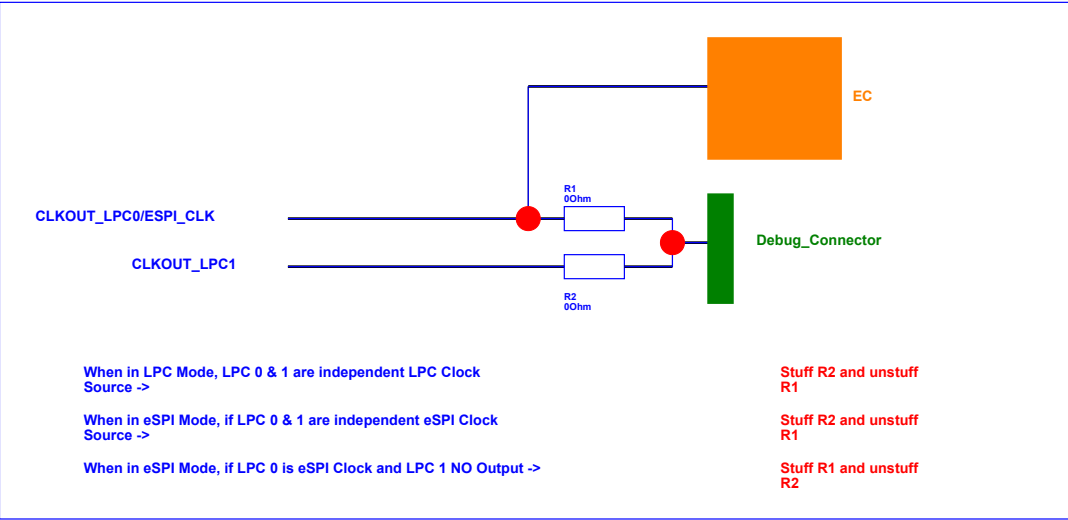
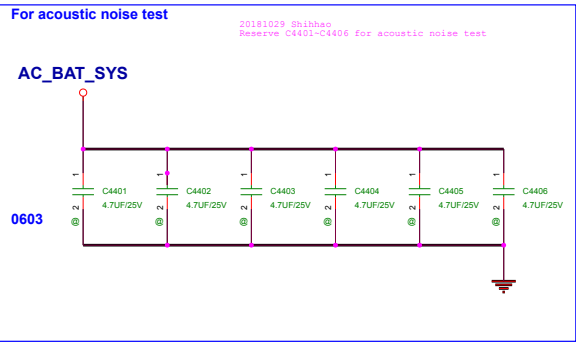
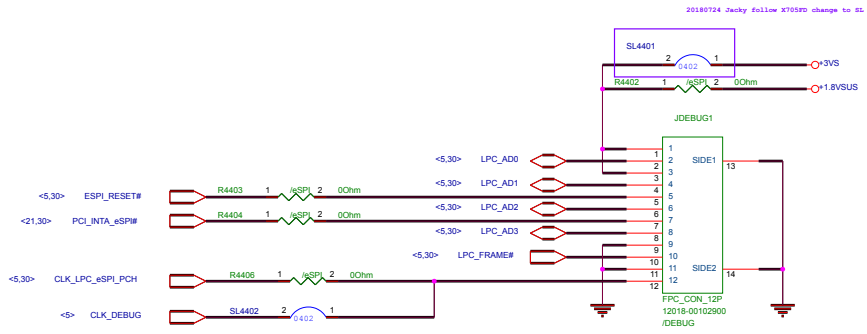
- 20181002 Shihhao
Change MB to IO connector pin define (move hall sensor to IO BD)
- 20181003 Shihhao
Change MB to IO connector pin define (move Audio Codec to IO BD)
- 20181011 Shihhao
Change MB to IO connector pin define (move Audio Codec to MB board & Audio Jack to IO board)
- 20181012 Shihhao
Change MB to IO connector pin define (move SPK connector to IO board)
- 20181022 Shihhao
Change MB to IO connector pin define (move speaker CONN to IO board & FAN CONN to MB)
- 20181019 Shihhao
Change MB to IO connector pin define (move FAN CONN to IO board & speaker CONN to MB)
- 20181106 Shihhao
Change MB to IO connector pin define
- 20181205 Shihhao
Change MB to IO connector pin define (add 2 pin for +5VSUS)

20181026 Shihhao
Reserve common choke for U2 (EMI request)



BOB		Project Name	Rev
ASUS		X409F	R1.0
Title : B to B Connector			
Size	Dept.:	ASUSTek	Engineer: NB3EE2
B	Date: Friday, February 22, 2019	Sheet	40 of 101

LPC Debug Port



When in LPC Mode, LPC 0 & 1 are independent LPC Clock
Source ->

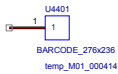
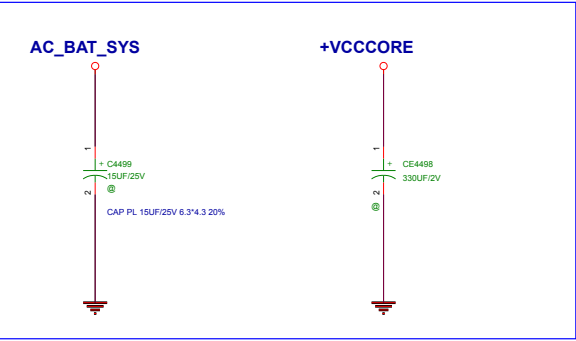
When in eSPI Mode, if LPC 0 & 1 are independent eSPI Clock
Source ->

When in eSPI Mode, if LPC 0 is eSPI Clock and LPC 1 NO Output ->

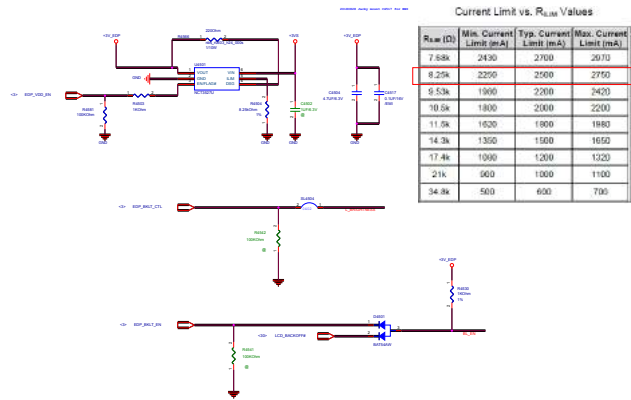
Stuff R2 and unstuff
R1

Stuff R2 and unstuff
R1

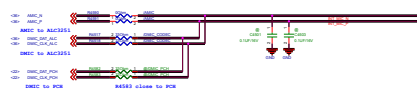
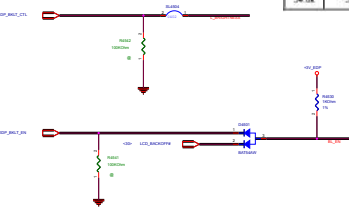
Stuff R1 and unstuff
R2



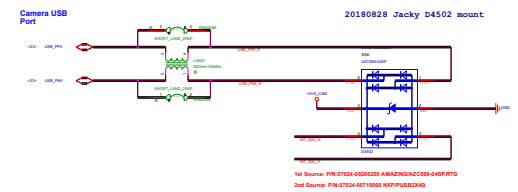
Project Name		Rev
ASUS X409F		R1.0
Title : DEBUG_LPC		
Size	Dept.: ASUSTek	Engineer: NB3EE2
B	Date: Friday, February 22, 2019	Sheet 44 of 101



$R_{OLIM} (\Omega)$	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
7.58k	2450	2700	2970
8.25k	2250	2500	2750
9.53k	1900	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1320	1500	1650
17.4k	1090	1200	1320
21k	900	1000	1100
34.8k	500	600	700

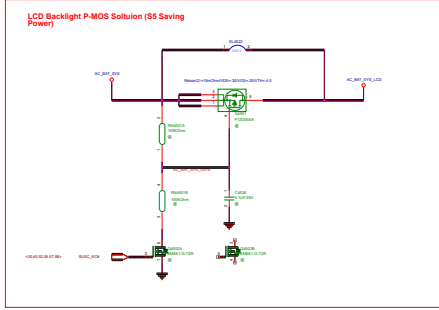
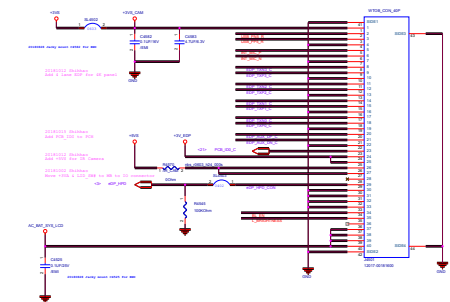
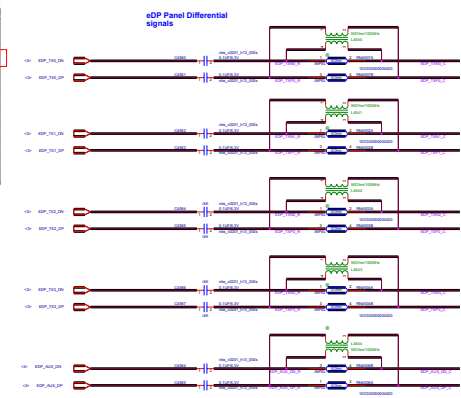


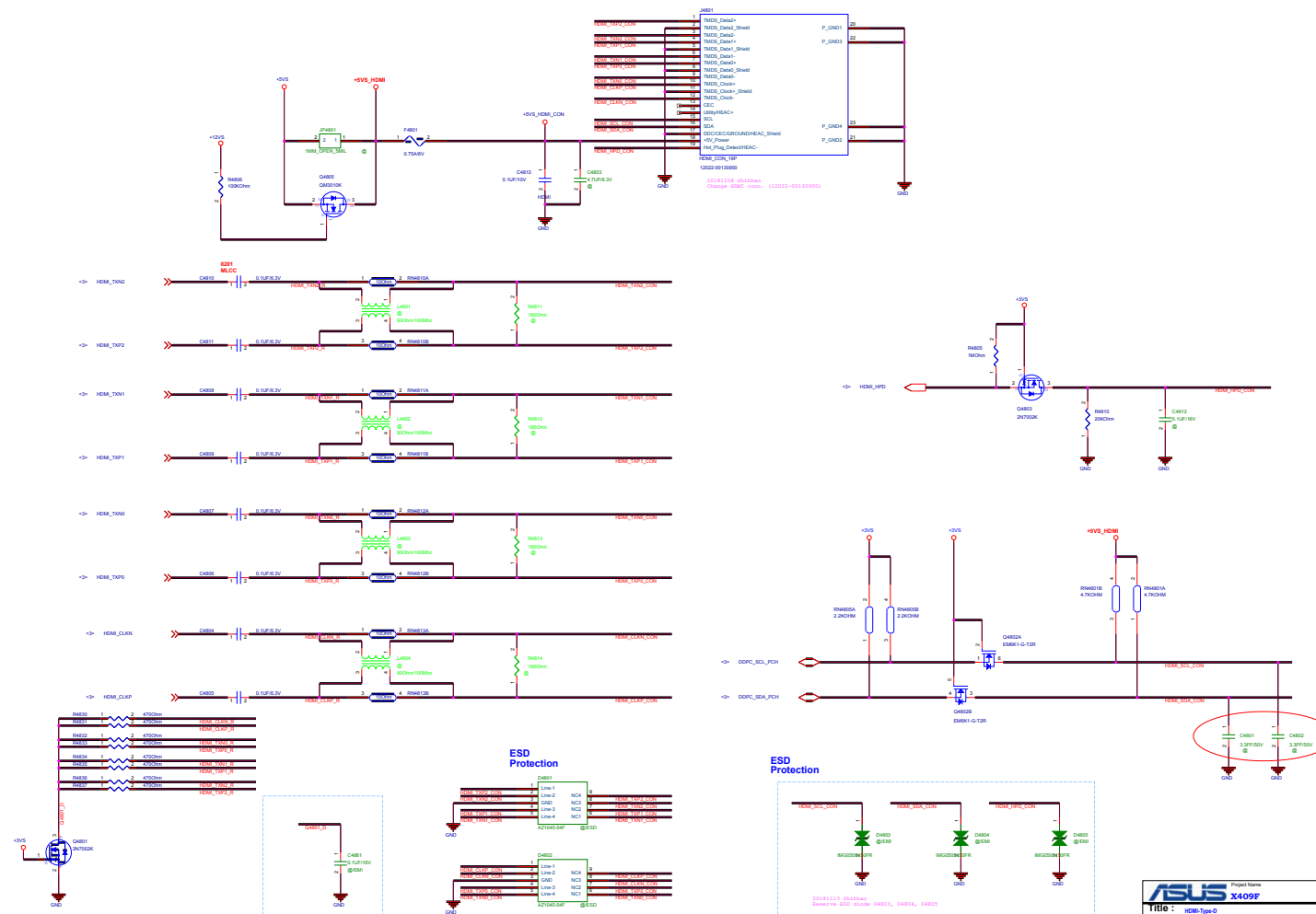
20180324 Brian
Add R4582/R4583 for DMIC to PCB.



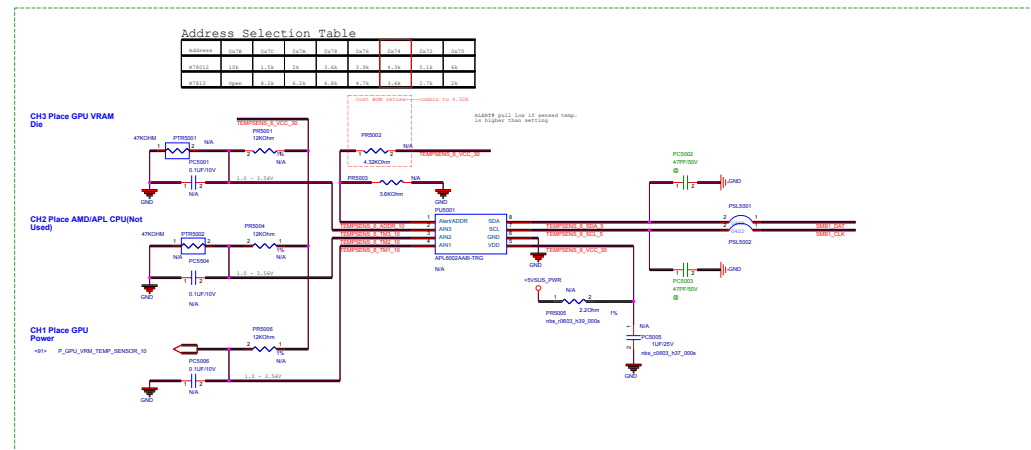
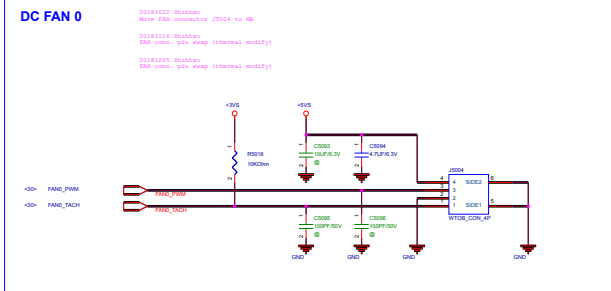
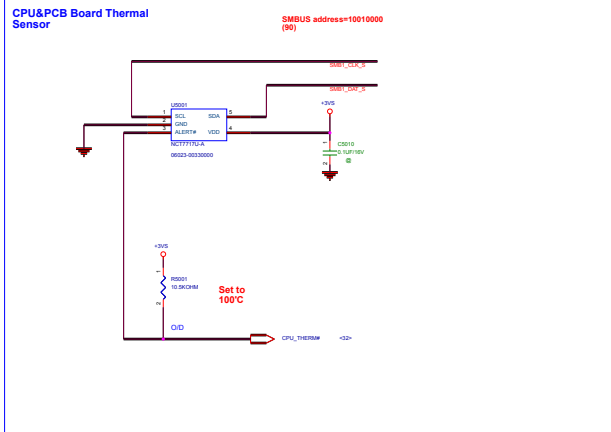
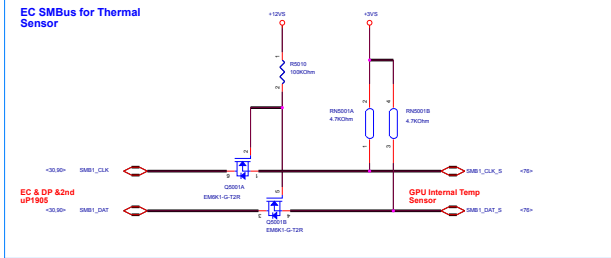
20180828 Jacky D4502 mount

1st Source: P/N:07024-0000000 AMAZINGAC000-0400-R70
2nd Source: P/N:07024-0070000 NBPUB00000

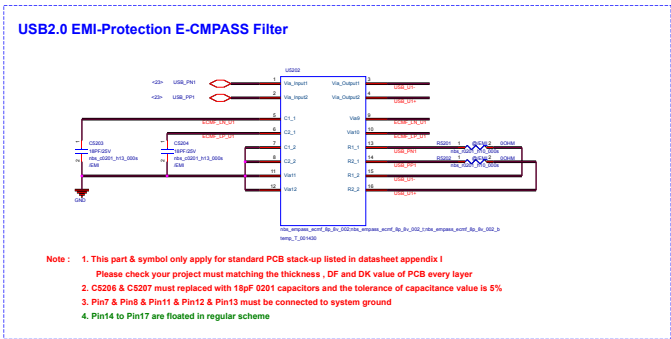
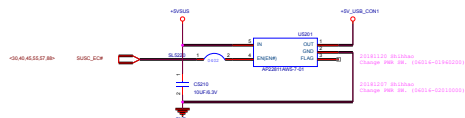
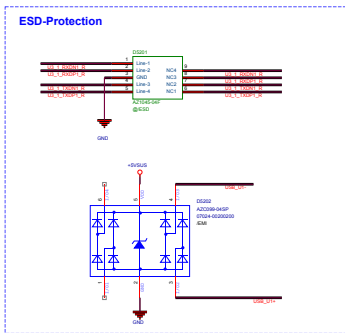
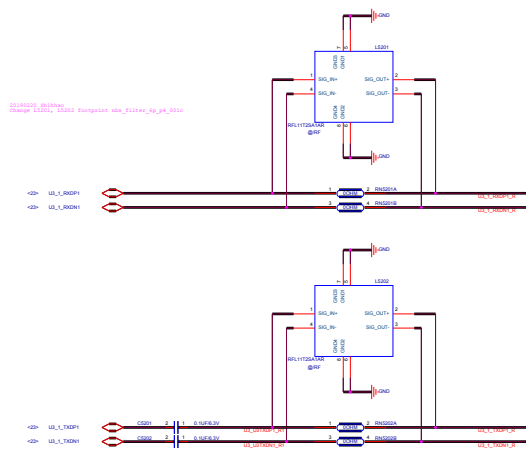




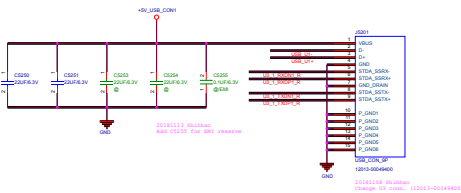
		Project Name		Rev
X409F				R1
Title : HDMI-Type-D				
Size	Dept.: ASUSTWK	Engineer:		NB3EE2
C				
Date: Friday, February 22, 2019		Chest	48	of 101

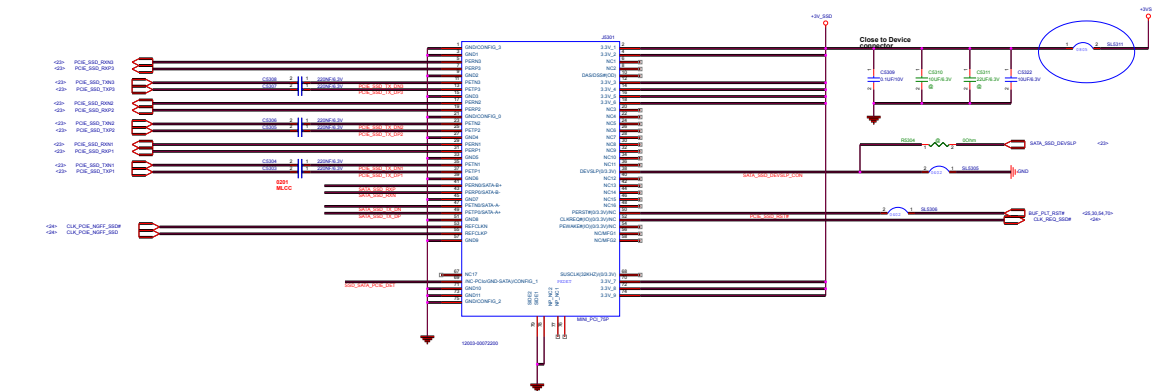


USB3.0_Port 0



1 - 0mm_05layer	0203AA11C18AA	Temp_T_001488
1 - 0mm_05layer	0203AA11C18AA	Temp_T_001489
1 - 0mm_05layer	0203AA11C18AA	Temp_T_001489
1 - 0mm_05layer	0203AA11C18AA	Temp_T_001489





36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

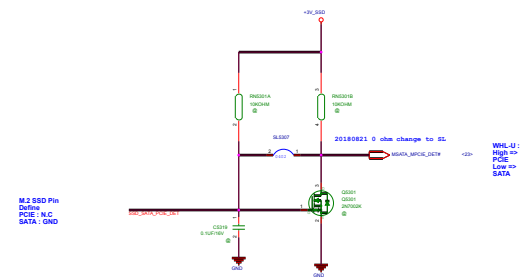
Table 36-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

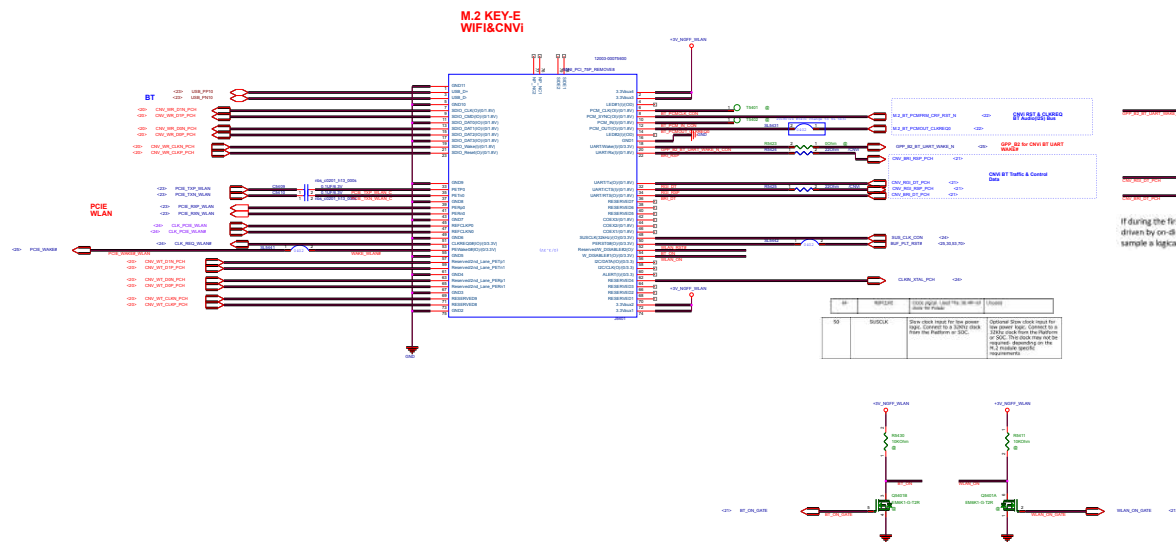
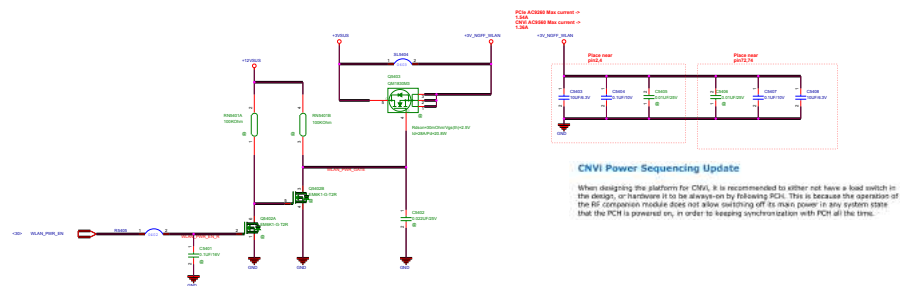
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2 / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer Chapter 3, "General Differential Signals Design Guidelines" * along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either PCIe* Gen2 devices or PCIe* Gen3 devices, follow the PCIe* Gen 3 / SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

For PCIe/SATA Auto Detect



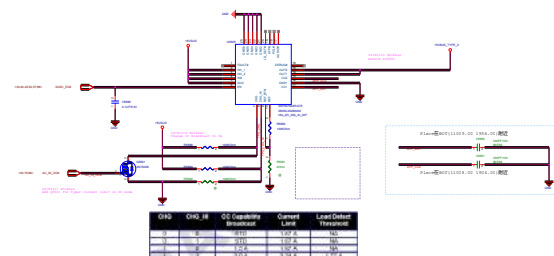
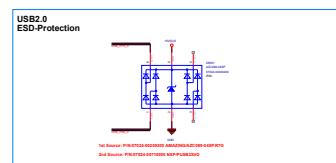
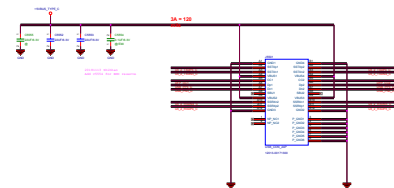
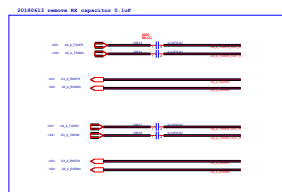
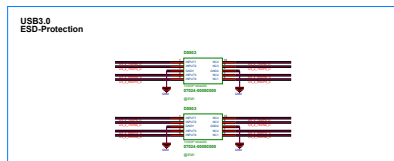
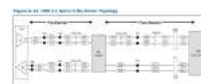
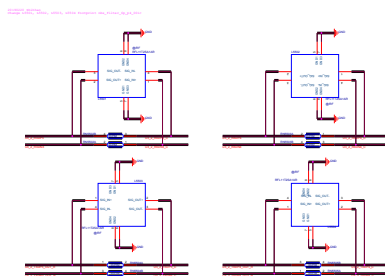


If during the first point above, if the CNVI does not exist, the CNVI_PCH_WAKE pin will be driven by on-die or platform pull-up resistors (typical 20K). In this case the strap will sample a logical high and the rest of the hardware process will not be performed.

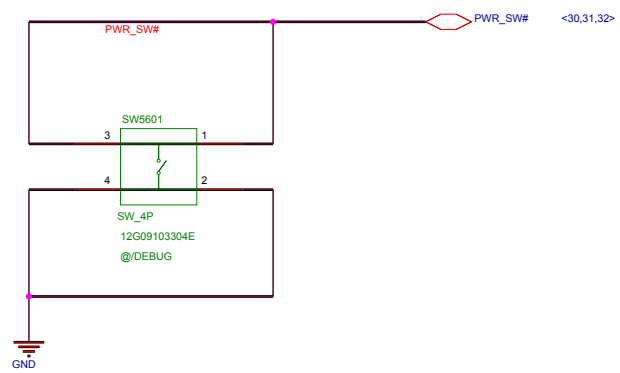
GPIO selectable function	
GPIO_32	0: UART_BT_WAKE output. Optional to connect to Bluetooth module's BT_WAKE pin. This is the recommended GPIO but other GPIOs can be selected for this function.
GPIO_34	0: BT_KILL output. Optional to connect to a Bluetooth module's BT_KILL pin on the Bluetooth module. This is the recommended GPIO but other GPIOs can be selected for this function.
GPIO_36	0: WLAN_KILL output. Optional to connect to a WLAN module's WLAN_KILL pin on the WLAN module. This is the recommended GPIO but other GPIOs can be selected for this function.
GPIO_C2	0: WLAN_WAKE output. Optional to connect to a WLAN module's WLAN_WAKE pin on the WLAN module. This is the recommended GPIO but other GPIOs can be selected for this function.
GPIO_C5	0: For CNVI: Unused. For CNVI: WLAN module's WLAN_WAKE pin on the WLAN module. This is the recommended GPIO but other GPIOs can be selected for this function.

Q With a PCIe card, we support to hard wake up by PME message when system in S0S. Link state at that time is L1.2. For a CNVI card, could you replace WAKE pin to WAKE pin in S0S? How does it work?

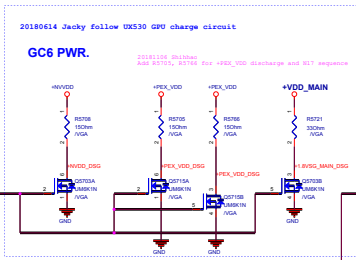
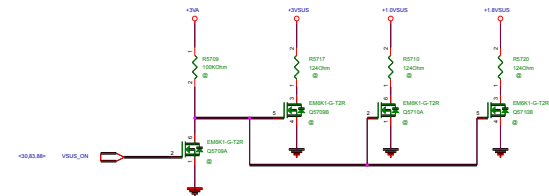
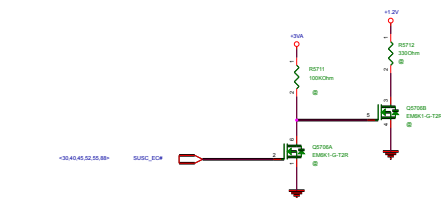
A It works the same, by in-band wake up by PME message. However, the message is sent over USB and not over PCIe.



PDE Dimension & Layers	Diffusion Model	AESE P-Value
1. 50m_Klayers	500/500/10/500/5	1.0e-5, 0.00000
1. 100m_Klayers	500/500/10/500/5	1.0e-5, 0.00000
1. 150m_Klayers	500/500/10/500/5	1.0e-5, 0.00000
1. 200m_Klayers	500/500/10/500/5	1.0e-5, 0.00000
1. 250m_Klayers	500/500/10/500/5	1.0e-5, 0.00000
1. 300m_Klayers	500/500/10/500/5	1.0e-5, 0.00000

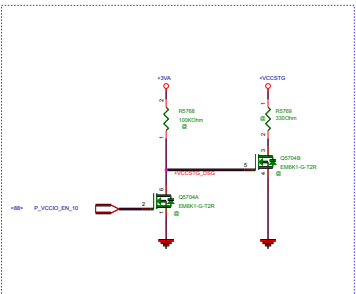


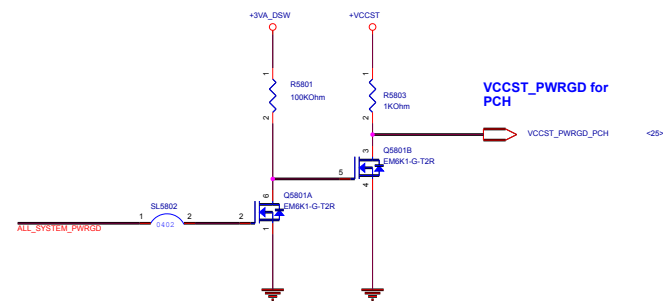
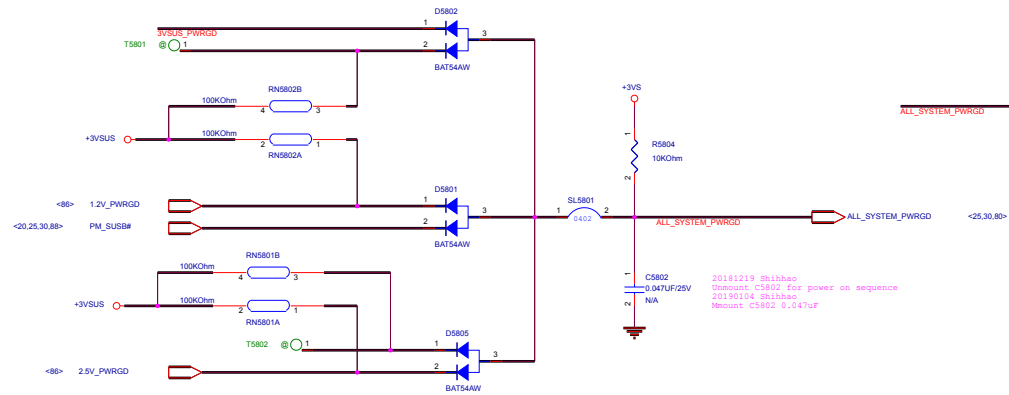
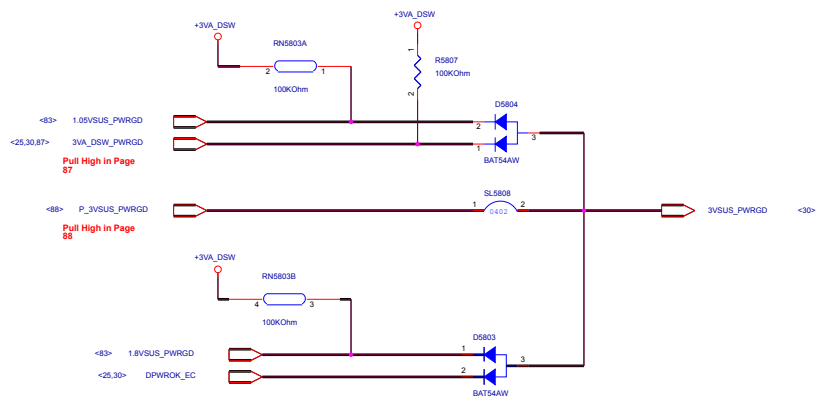
Main Board



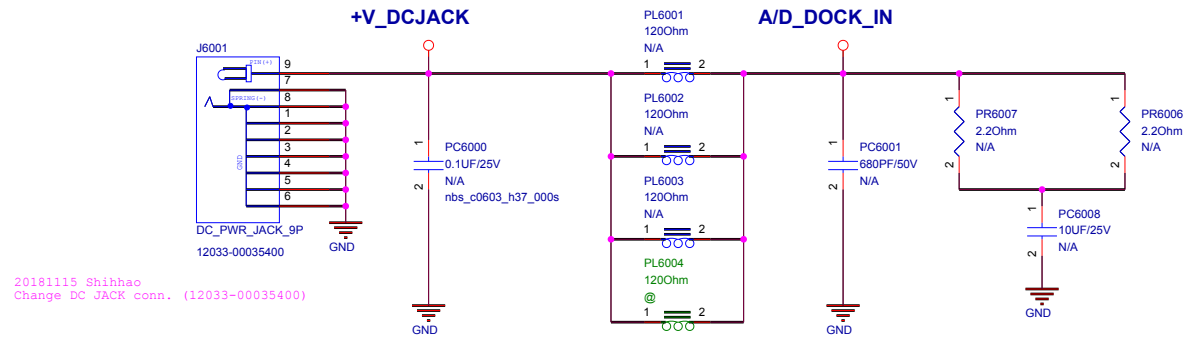
2018/01/03 Jack Change Q5703 mount, R5708 change 15ohm for N17S sequence.

2018/01/05 Jack Change R5705 from 15 ohm to 2.2 ohm for N17S sequence

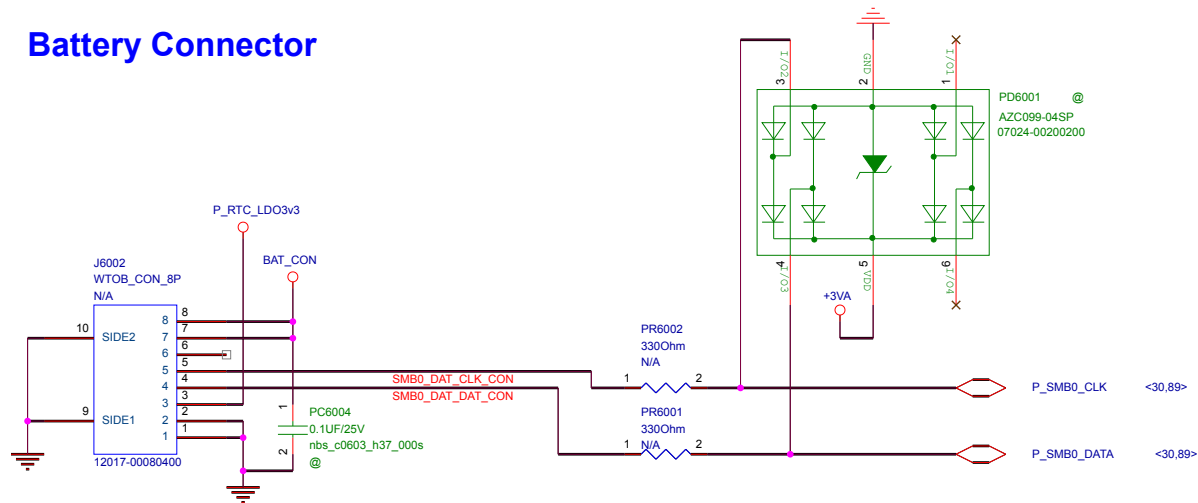




DC Jack

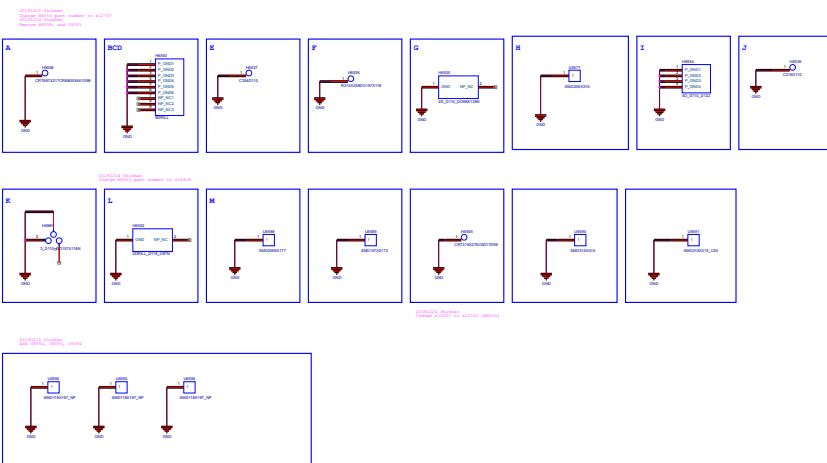


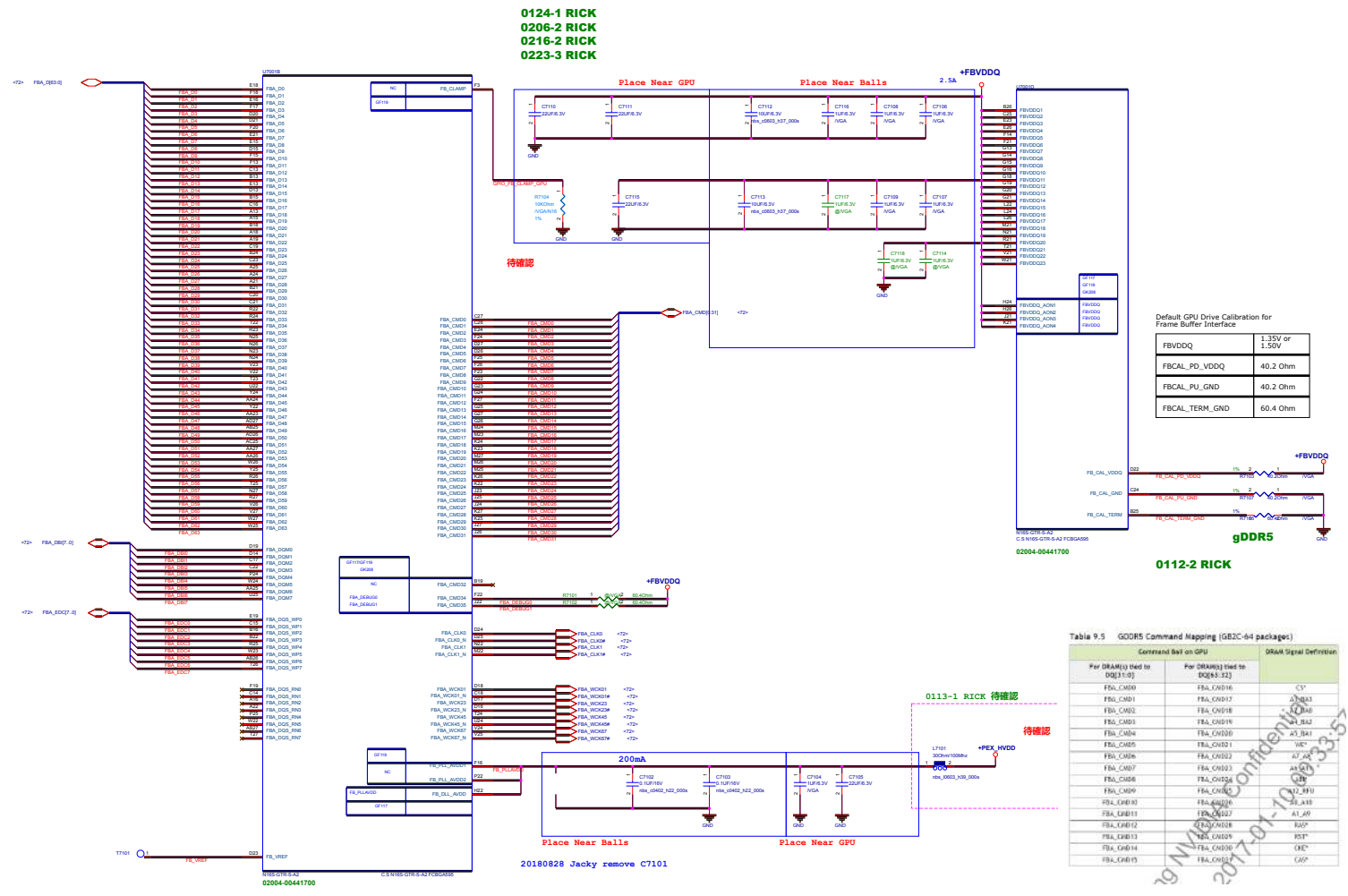
Battery Connector

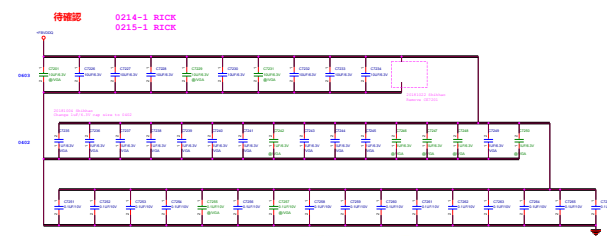
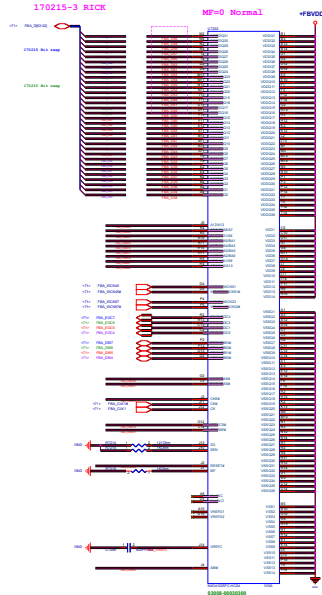
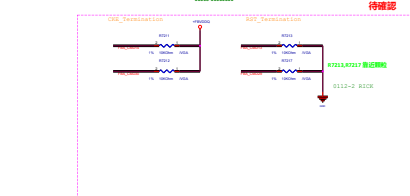


<Variant Name>

ASUS		Project Name	Rev
Title :		R1.0	
Size	Dept.: ASUS	Engineer:	
A	Date: Friday, February 22, 2019	Sheet	60 of 101





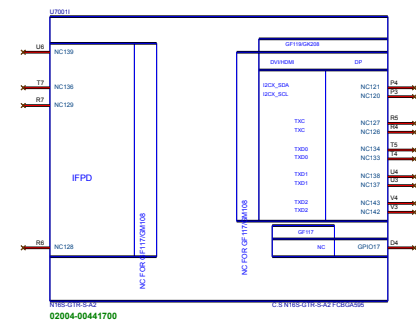
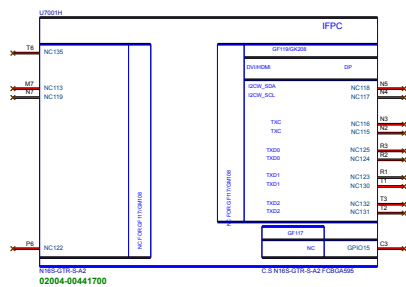
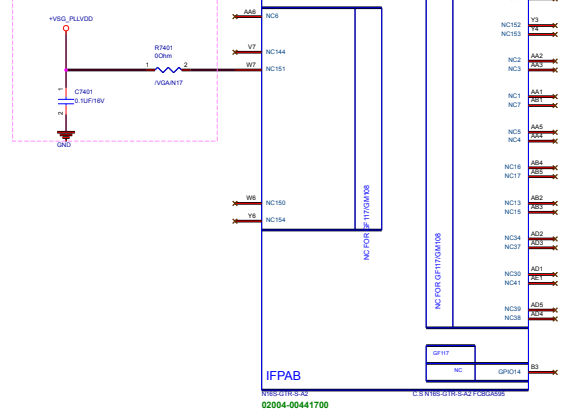
[illegible]

Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For N17x GPU Package: 082C-04 (preliminary)			
1.0 μ F	0402 [0402]	8	Under GPU PBGA/GPBGA ball in evenly distributed throughout partition
10 μ F	0402 [0402]	2	
10 μ F	0402 [0402]	1	Near GMI device
22 μ F	0402 [0402]	3	

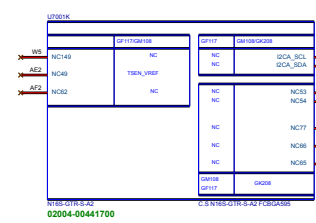
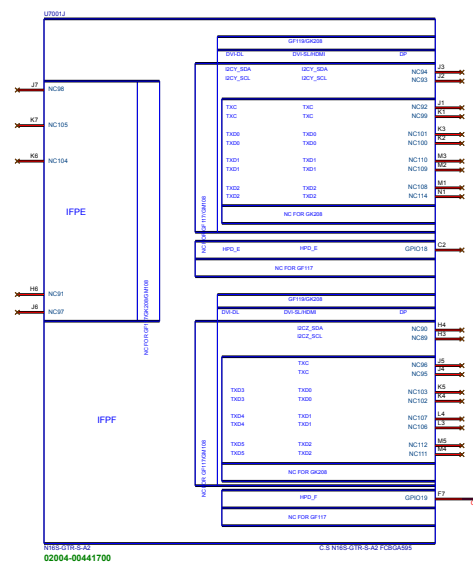
[illegible]

LVDS

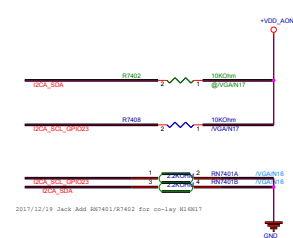
0221-3 RICK



CRT



0213-2 RICK
0216-3 RICK

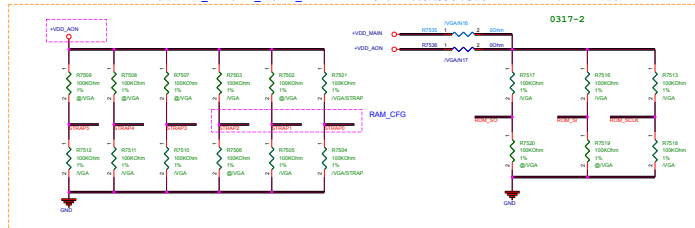


BOM		Project Name	Rev
ASUS		X409F	R1.0
Title :		VGA, NV, N16S-GTR, DISPLAY	
Size	Dept.:	ASUS	Engineer: NB3EE2
C			

VGA_DEVICE = 0
PCIE_CFG = 0
DEVID_CFG = 0
SMB_ALT_ADDR = 0

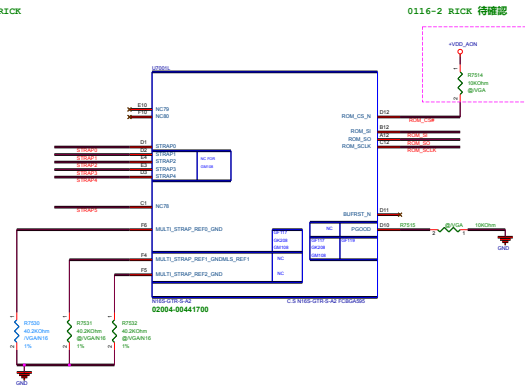
	N17S-G0,G2 GDDR5		N16V-GMR1, GDDR5
Strap Pin	MT51J25M32H-80B 03008-00051600 (b4d)	HYNIX26P30 H5GCB24AJR-R2C 03008-00052000 (b4d)	MT51J25M32H-70B 03008-00051700 (b4d)
STRAP0	L: R7504 = 100kohm	R: R7501 = 100kohm	R7501 = 43.9kohm, R7504=--@
STRAP1	L: R7505 = 100kohm	L: R7505 = 100kohm	Do not stuff
STRAP2	R: R7503 = 100kohm	R: R7503 = 100kohm	Do not stuff
STRAP3		L: R7510 = 100kohm	Do not stuff
STRAP4		L: R7511 = 100kohm	Do not stuff
STRAP5		L: R7512 = 100kohm	Do not stuff
ROM_SO	R: R7517 = 100kohm		R7517 = 4.99kohm, R7520=--@
ROM_SI	R: R7516 = 100kohm		R7516 = 4.99kohm, R7519=--@
ROM_SCLK	R: R7513, R7518 = 100kohm		R7518 = 4.99kohm, R7513=--@

設定 ROM_SCLK, ROM_SI, ROM_SO PULL DOWN, 與nv確認是否可以使用 SW override, FAE :建議DISABLE



Strap Pin	Strap Pin	Strap Pin	Strap Pin	Strap Pin	Strap Pin	Strap Pin	Strap Pin	Strap Pin	Strap Pin
STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	STRAP5	STRAP6	STRAP7	STRAP8	STRAP9
STRAP10	STRAP11	STRAP12	STRAP13	STRAP14	STRAP15	STRAP16	STRAP17	STRAP18	STRAP19
STRAP20	STRAP21	STRAP22	STRAP23	STRAP24	STRAP25	STRAP26	STRAP27	STRAP28	STRAP29
STRAP30	STRAP31	STRAP32	STRAP33	STRAP34	STRAP35	STRAP36	STRAP37	STRAP38	STRAP39
STRAP40	STRAP41	STRAP42	STRAP43	STRAP44	STRAP45	STRAP46	STRAP47	STRAP48	STRAP49
STRAP50	STRAP51	STRAP52	STRAP53	STRAP54	STRAP55	STRAP56	STRAP57	STRAP58	STRAP59
STRAP60	STRAP61	STRAP62	STRAP63	STRAP64	STRAP65	STRAP66	STRAP67	STRAP68	STRAP69
STRAP70	STRAP71	STRAP72	STRAP73	STRAP74	STRAP75	STRAP76	STRAP77	STRAP78	STRAP79
STRAP80	STRAP81	STRAP82	STRAP83	STRAP84	STRAP85	STRAP86	STRAP87	STRAP88	STRAP89
STRAP90	STRAP91	STRAP92	STRAP93	STRAP94	STRAP95	STRAP96	STRAP97	STRAP98	STRAP99

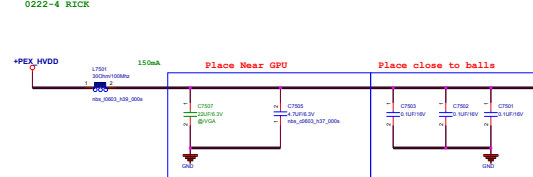
0208-2 RICK



0116-2 RICK 待確認

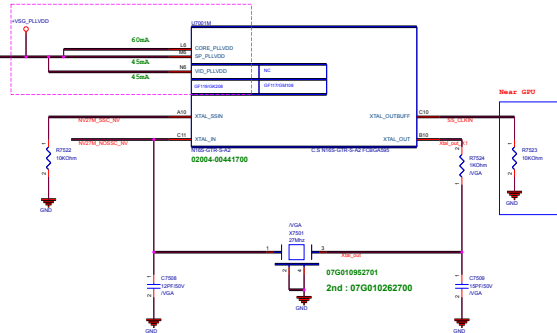
Xtal

0222-4 RICK



0113-1 RICK

0216-5 RICK



2017/12/27 Jack C7608 change 13p.

ASUS	Project Name	Rev
X409F		01.0
Title : VGA.W. M16S-GTR ROMXtal		
Dept: ASUS	Engineer: NB3EE2	
Date: Friday, February 02, 2018	Draw: TS	of 100

GPIO TEMP SENSOR, JTAG

Table 14.1 GPIO Descriptions for GBC-64 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	WDOG_PWN	O	PWM output to control WDOG	0 to 1V _{DD} PWN
GPIO1	GCAM_GCA_RST_N	O	FB enable for GC62.3	Open Source 10 kΩ pull-down

Table 14.1 GPIO Descriptions for GBC-64 Packages (Continued)

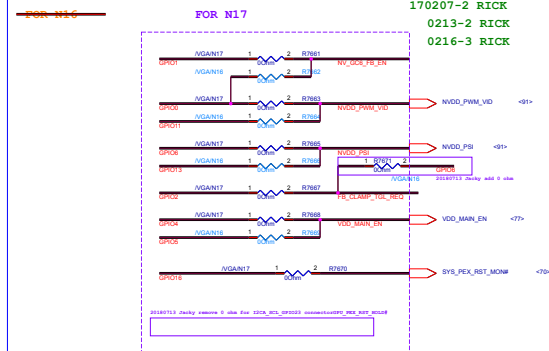
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO2	GCAM_GPU_STBYT??	I	GPU wake signal for GC62.3	10 kΩ pull-up to 1V _{DD} , unless driven actively
GPIO3	WDOG_PWN	O	Pulse output to control the WDOG power supply	0 to 1V _{DD} output
GPIO4	GCAM10E_ANAL_IN	O	Open Drain, 10 kΩ pull-up to 1V _{DD}	Open Drain 10 kΩ pull-up to 1V _{DD}
GPIO5	Flash_LOCK	I	Active Low Flash Lock	10 kΩ pull-up to 1V _{DD}
GPIO6	WDOG_RST	O	Pulse output to control WDOG	0 to 1V _{DD} output
GPIO7	LED_BL_PWM	O	Pulse Backlight enable	100 kΩ pull-down
GPIO8	WDOG_RST_CTL	O	Memory controller control	100 kΩ pull-down
GPIO9	THERM_ALERT1	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V _{DD}
GPIO10	WDOG_RST_CTL	O	Memory WREF Control	100 kΩ pull-down
GPIO11	LED_VDD	O	Quadruple Enable	100 kΩ pull-down
GPIO12	Flash_LOCK	I	Active Low Flash Lock	100 kΩ pull-up to 1V _{DD}
GPIO13	LED_BL_PWM	O	LED Backlight Enable	100 kΩ pull-down
GPIO14	HOT_PLUG	I	Hot Plug Detect for if PPS	Inverted input, See Figure 14.3
GPIO15	HOT_PLUG	I	Hot Plug Detect for if PPS	Inverted input, See Figure 14.3
GPIO16	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven
GPIO17	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven
GPIO18	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven

Table 14.1 GPIO Descriptions for GBC-64 Packages (Continued)

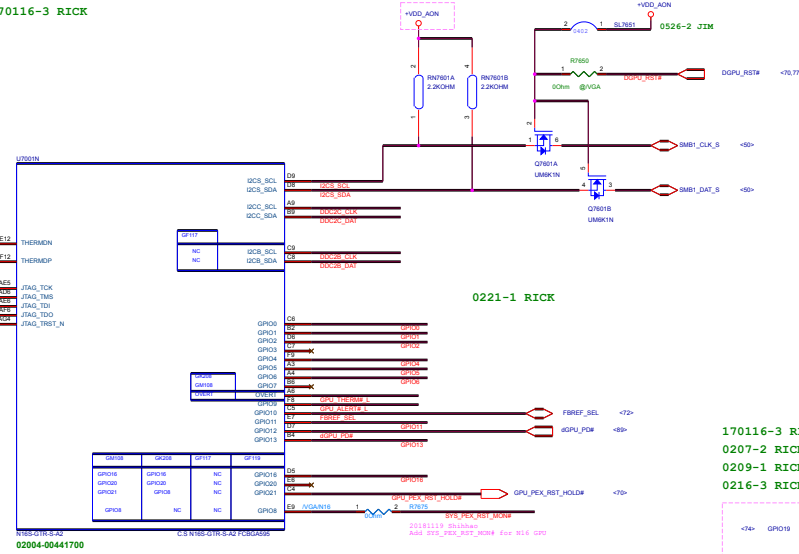
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO19	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven
GPIO20	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven
GPIO21	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven
GPIO22	WDOG_RST_CTL	O	System side PPS reset	10 kΩ pull-up to 1V _{DD} , unless actively driven

un-used:

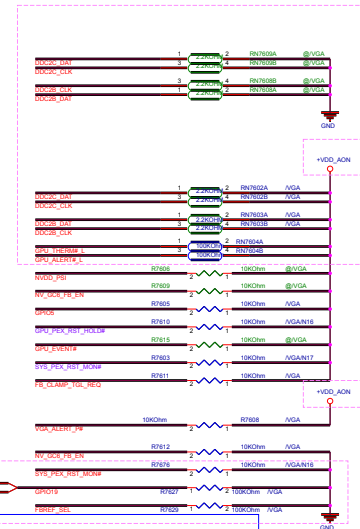
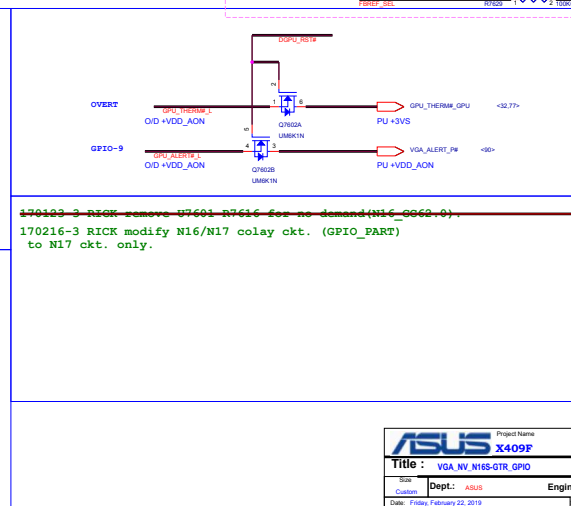
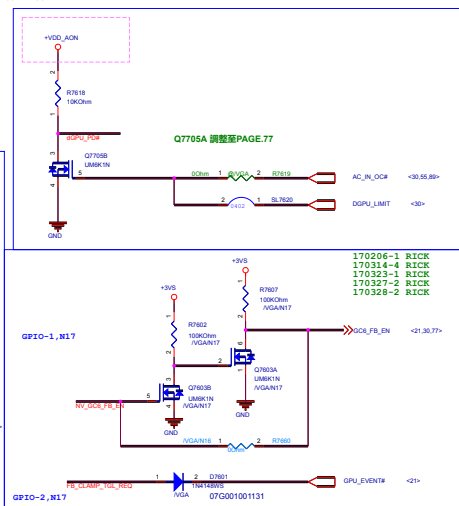
GPIO-3
GPIO-5
GPIO-7
GPIO-8
GPIO-11
GPIO-13
GPIO-14
GPIO-15
GPIO-17
GPIO-18
GPIO-19
GPIO-20
GPIO-21
GPIO-22



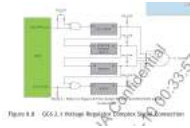
170116-3 RICK



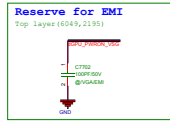
170116-3 RICK
0207-2 RICK
0209-1 RICK
0216-3 RICK



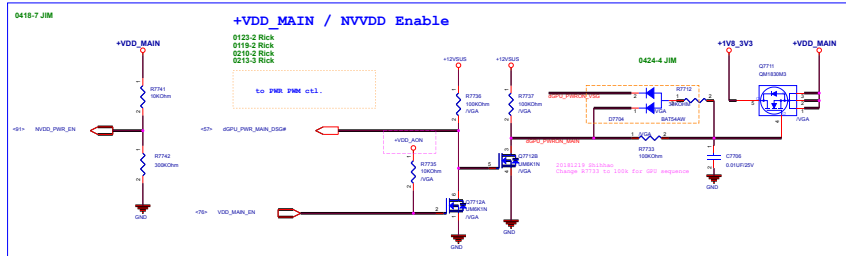
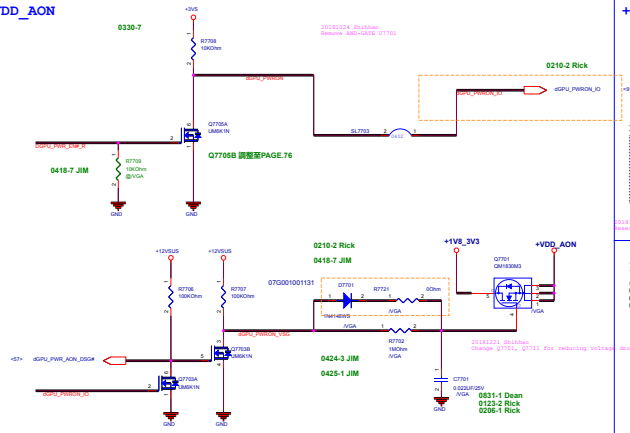
dGPU Power Sequence



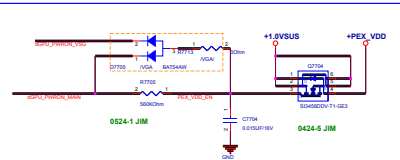
170112-RICK
0202-2 Dean



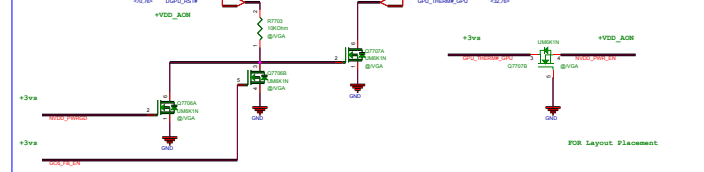
+VDD_AON



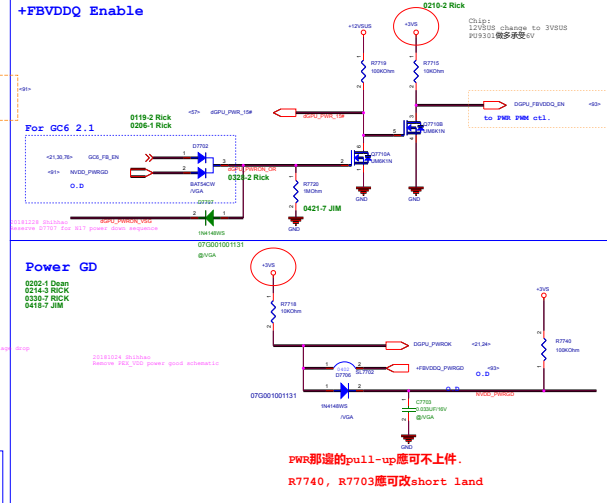
+PEX_VDD



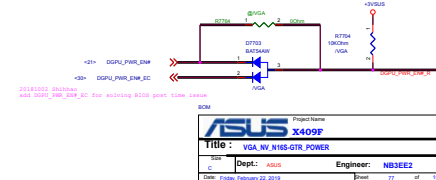
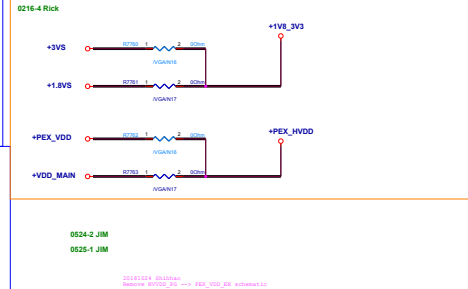
NVDD POWER GOOD LOOPBACK ref.G753VI

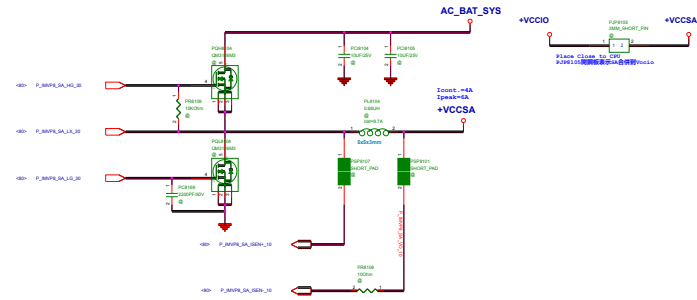
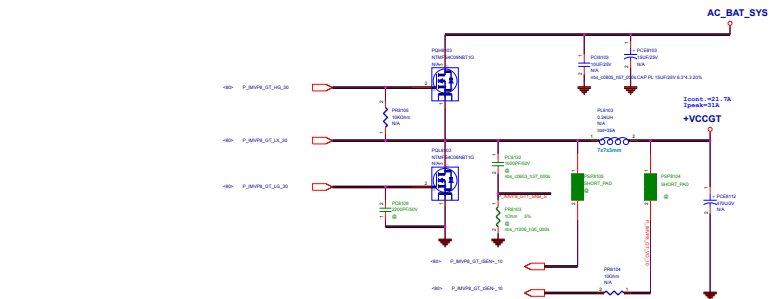
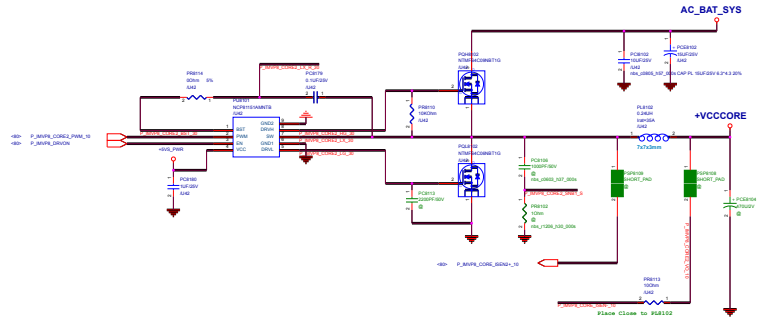
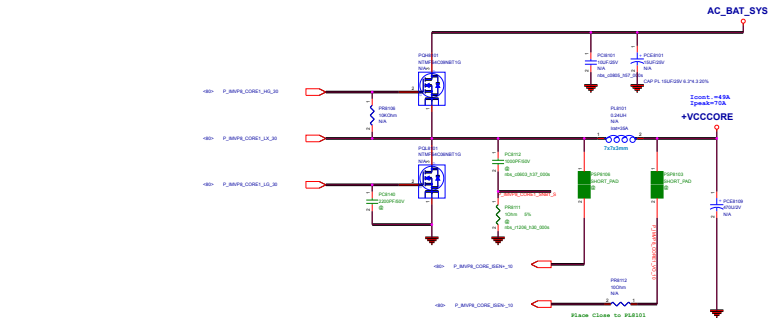


+FBVDDQ Enable



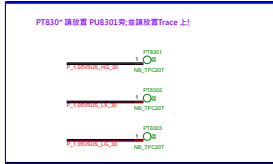
N16/N17 power source :

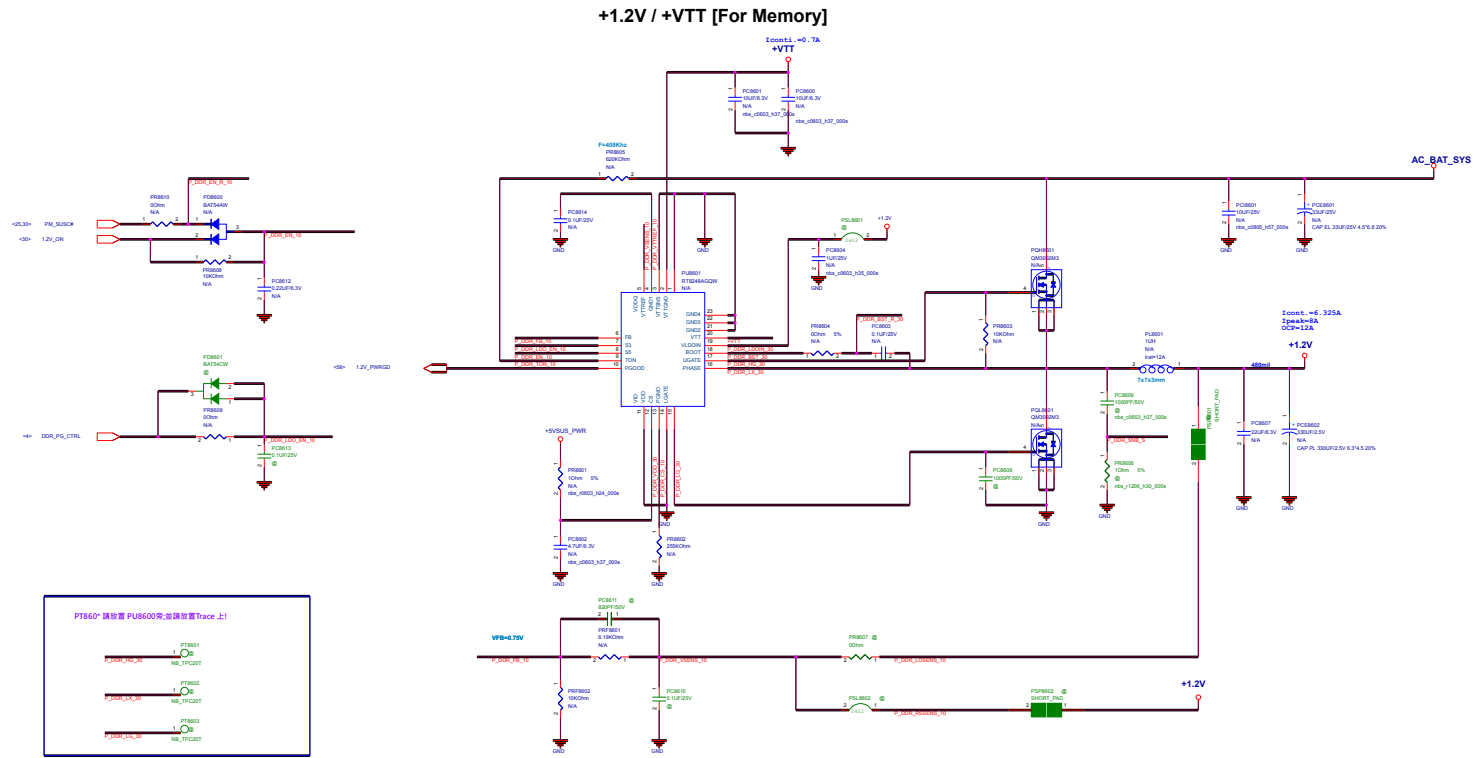


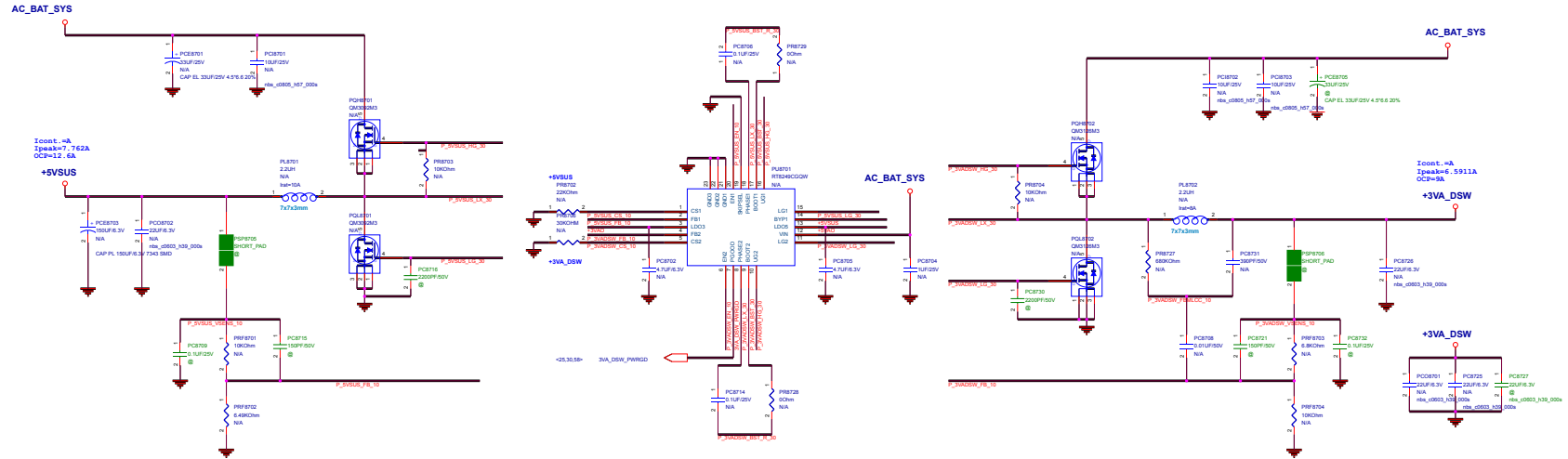


ASUS		Project Name	Rev
H100			010
Part:	Rev:	Engineer:	Non
Date: 2024/01/01		Drawn:	01

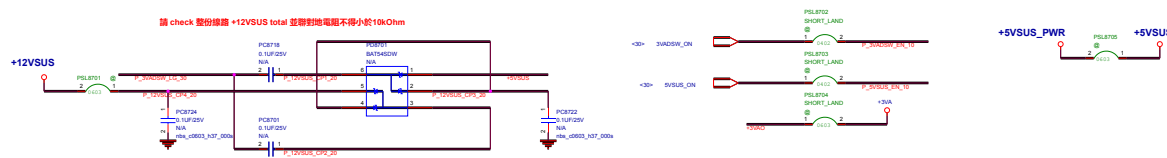
+1.05VSUS [For PCH]







請 check 整個線路 +12VSUS total 並聯到地電阻不得小於10kOhm



PT8701 請放置 PU8701旁,並請放置Trace上!

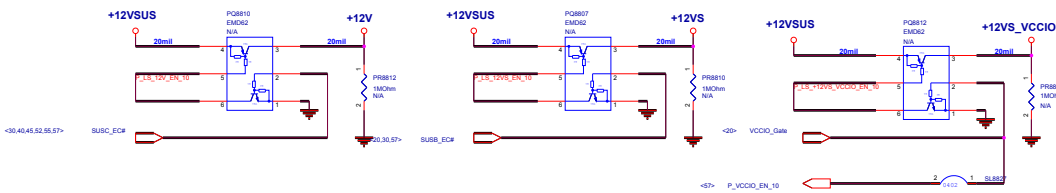
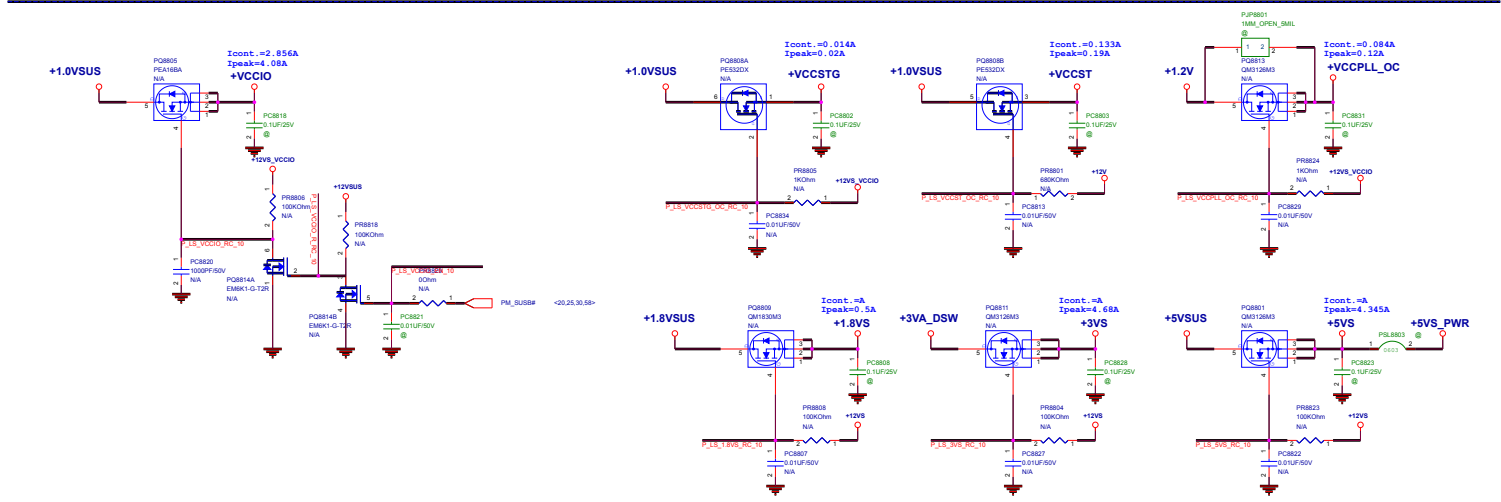



Adaptor Mode (MVP8)

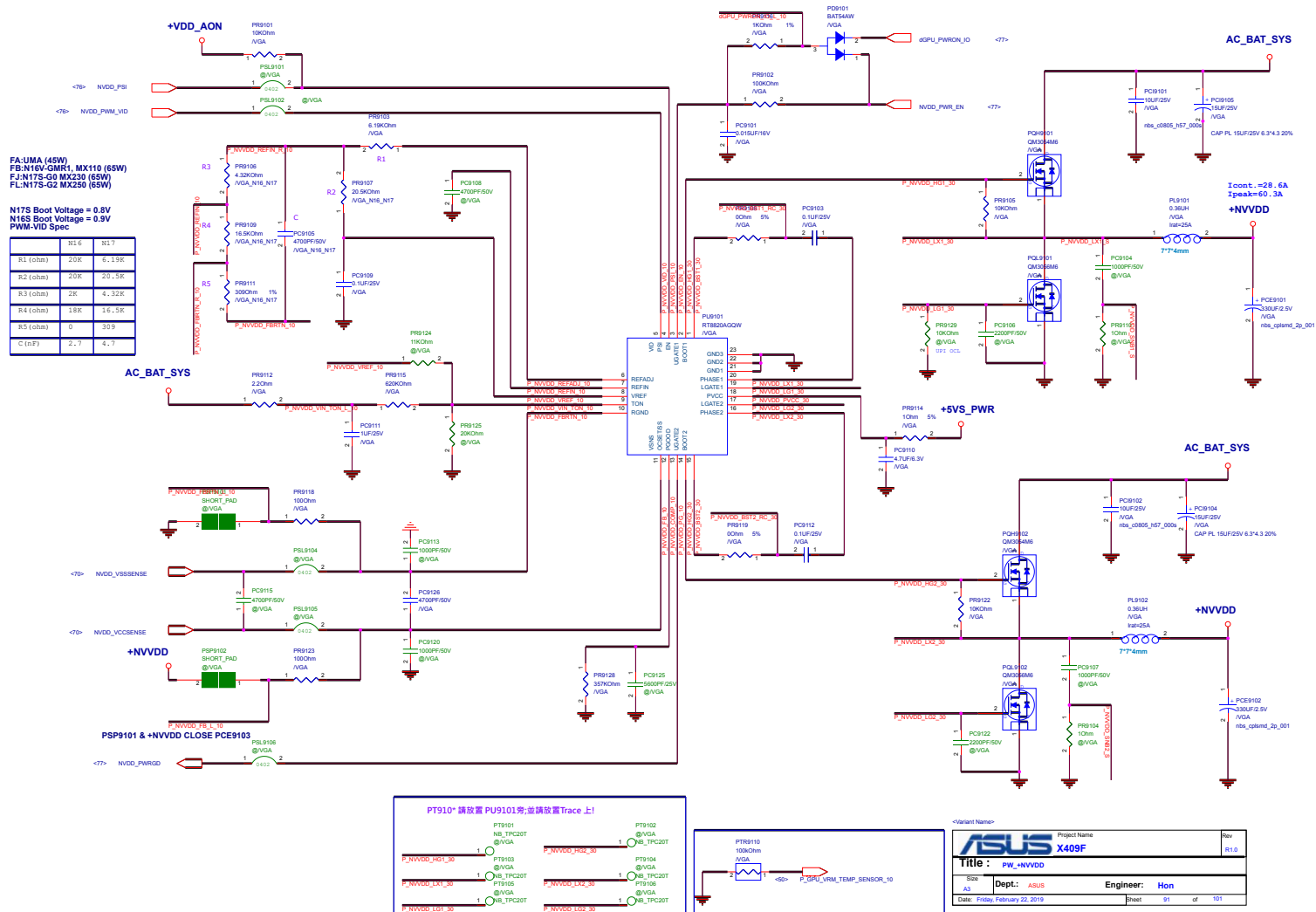
	S5	S3	S33	S4	S8	S8 with USB Charger+
PS_ON	1	1	1	1	1	1
3VADSW_ON	1	1	1	1	1	1
3VSUS_ON	1	1	1	1	1	1
5VSUS_ON	1	1	1	1	1	1
1.8V_ON	1	1	1	1	1	1
SUSC_ECP	1	1	1	1	1	1
SUSB_ECP	1	1	1	1	1	1

Battery Mode (MVP8)

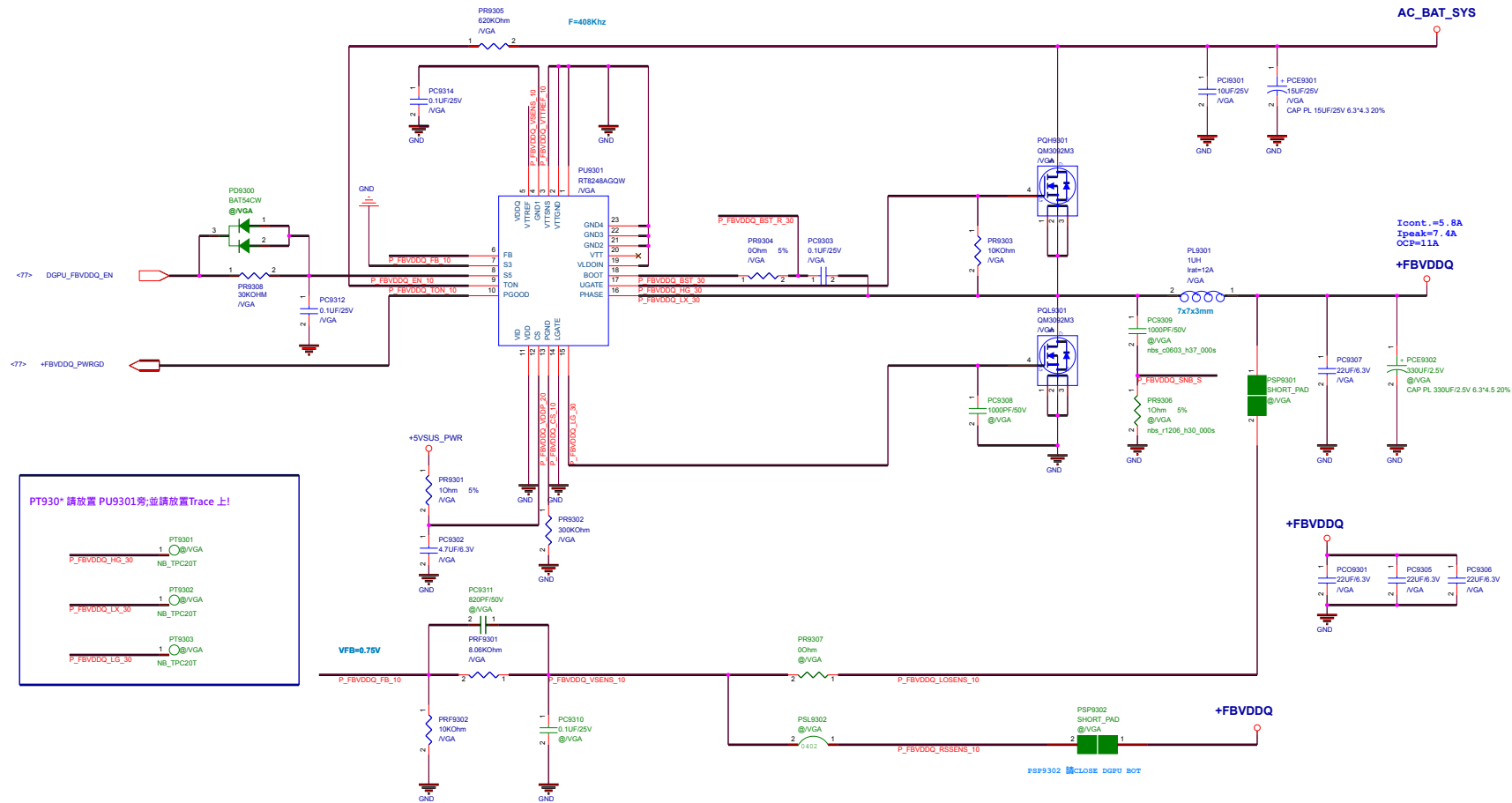
	S5	S3	S33	S4	S8	S8 with USB Charger+
PS_ON	1	1	1	1	1	1
3VADSW_ON	1	1	1	1	1	1
3VSUS_ON	1	1	1	1	1	1
5VSUS_ON	1	1	1	1	1	1
1.8V_ON	1	1	1	1	1	1
SUSC_ECP	1	1	1	1	1	1
SUSB_ECP	1	1	1	1	1	1




		Project Name	Rev
Title : PW_LOAD_SWITCH		R1.0	
Size A3	Dept.: ASUS	Engineer:	
Date: Friday, February 22, 2019		Sheet 88 of 102	

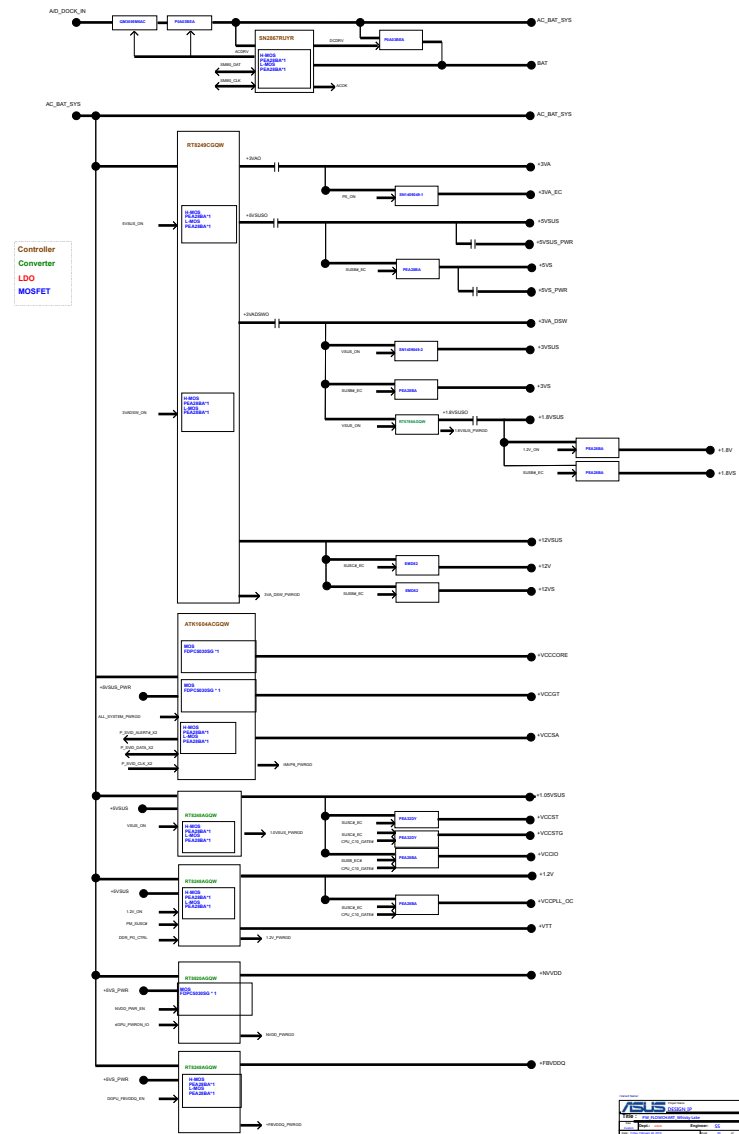


+FBVDDQ [For VRAM]



«Core Design»

		Project Name X409F	Rev R1.0
Title : PW_+FBVDQD			
Size A3	Dept.: NB Power team		Engineer: Hon
Date: Friday, February 22, 2019		Sheet 93 of 103	





X705FD Power On Sequence - DC mode

